

SBFS026B − JUNE 2004 − REVISED SEPTEMBER 2007

4-Channel, Asynchronous Sample Rate Converter

FEATURES

- AUTOMATIC SENSING OF INPUT-TO-OUTPUT SAMPLING RATIO
- WIDE INPUT-TO-OUTPUT SAMPLING RANGE: 16:1 to 1:16
- SUPPORTS INPUT AND OUTPUT SAMPLING RATES UP TO 212kHz
- DYNAMIC RANGE: 128dB (−60dbFS Input, BW = 20Hz to f_S/2, A-Weighted)
- THD+N: −125dB (0dbFS Input, BW = 20Hz to f_S/2)
- HIGH-PERFORMANCE, LINEAR PHASE DIGITAL FILTERING
- FLEXIBLE AUDIO SERIAL PORTS:
  - Master or Slave Mode Operation
  - Supports I^2S, Left-Justified, Right-Justified, and TDM Data Formats
  - TDM Mode Allows Daisy-Chaining of Up to Four Devices
- SUPPORTS 24-, 20-, 18-, or 16-BIT INPUT AND OUTPUT DATA:
  - All Output Data is Dithered from the Internal 28-Bit Data Path
- SERIAL PERIPHERAL INTERFACE (SPI)™ PORT SUPPORTS REGISTER READ AND WRITE OPERATIONS IN SOFTWARE MODE
- BYPASS MODE:
  - Routes Input Port Data Directly to the Output Port
- FOUR GROUP DELAY OPTIONS FOR THE INTERPOLATION FILTER
- DIRECT DOWNSAMPLING OPTION FOR THE DECIMATION FILTER
- DIGITAL DE-EMPHASIS FILTER:
  - User-Selectable for 32kHz, 44.1kHz, and 48kHz Sampling Rates
- SOFT MUTE FUNCTION
- PROGRAMMABLE DIGITAL OUTPUT ATTENUATION (SOFTWARE MODE ONLY):
  - 256 Steps: 0dB to −127.5dB with 0.5dB Steps
- INPUT-TO-OUTPUT SAMPLING RATIO READBACK (SOFTWARE MODE ONLY)
- POWER-DOWN MODES
- SUPPORTS OPERATION FROM A SINGLE +1.8V OR +3.3V POWER SUPPLY
- AVAILABLE IN A TQFP-64 PACKAGE

APPLICATIONS

- DIGITAL MIXING CONSOLES
- DIGITAL AUDIO WORKSTATIONS
- AUDIO DISTRIBUTION SYSTEMS
- BROADCAST STUDIO EQUIPMENT
- GENERAL DIGITAL AUDIO PROCESSING

DESCRIPTION

The SRC4184 is a four-channel, asynchronous sample rate converter (ASRC), designed for professional and broadcast audio applications. The SRC4184 combines a wide input-to-output sampling ratio with outstanding dynamic range and ultra low distortion. The input and output serial ports support the most common audio data formats, as well as a time division multiplexed (TDM) format. This allows the SRC4184 to interface to a wide range of audio data converters, digital audio receivers and transmitters, and digital signal processors.

The SRC4184 may be operated in Hardware mode as a standalone pin-programmed device, with dedicated control pins for serial port mode, audio data format, soft mute, bypass, and digital filtering functions. Alternatively, the SRC4184 may be operated in Software mode, where a four-wire serial peripheral interface (SPI) port provides access to internal control and status registers.

The SRC4184 operates from either a +1.8V core supply or a +3.3V core supply. When operating from +3.3V, the +1.8V required by the core logic is derived from an internal voltage regulator. The SRC4184 also requires a digital I/O supply, which operates from +1.65V to +3.6V. The SRC4184 is available in a TQFP-64 package.

U.S. Patent No. 7,262,716.

ABSOLUTE MAXIMUM RATINGS(1)

Core Supply Voltage	
VDD18	−0.3V to +2.0V
VDD33	−0.3V to +4.0V
Digital I/O Supply Voltage, V_{IO}	−0.3V to +4.0V
Digital Input Voltage	−0.3V to +4.0V
Operating Case Temperature Range, T_C	−40°C to +85°C
Storage Temperature Range, T_{STG}	−65°C to +150°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet.

ELECTRICAL CHARACTERISTICS

All specifications at T_A = +25°C, VDD33 = +3.3V, V_{IO} = +3.3V, REGEN = High, and VDD18 floating, unless otherwise noted.

PARAMETER	CONDITIONS	SRC4184 MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE					
Resolution			24		Bits
Input Sampling Frequency, f_{SIN}		4		212	kHz
Output Sampling Frequency, f_{SOUT}		4		212	kHz
INPUT/OUTPUT SAMPLING RATIO					
Upsampling				1:16	
Downsampling				16:1	
DYNAMIC RANGE	BW = 20Hz to f_{SOUT}/2, −60dBFS Input f_{IN} = 1kHz, A-Weighted				
44.1kHz:48kHz			128		dB
48kHz:44.1kHz			128		dB
48kHz:96kHz			128		dB
44.1kHz:192kHz			128		dB
96kHz:48kHz			128		dB
192kHz:12kHz			128		dB
192kHz:32kHz			128		dB
192kHz:48kHz			128		dB
32kHz:48kHz			128		dB
12kHz:192kHz			128		dB
TOTAL HARMONIC DISTORTION + NOISE	BW = 20Hz to f_{SOUT}/2, −60dBFS Input f_{IN} = 1kHz, Unweighted				
44.1kHz:48kHz			−125		dB
48kHz:44.1kHz			−125		dB
48kHz:96kHz			−125		dB
44.1kHz:192kHz			−125		dB
96kHz:48kHz			−125		dB
192kHz:12kHz			−125		dB
192kHz:32kHz			−125		dB
192kHz:48kHz			−125		dB
32kHz:48kHz			−125		dB
12kHz:192kHz			−125		dB
Interchannel Gain Mismatch			0		dB
Interchannel Phase Deviation			0		degrees

(1) Dynamic performance is measured with an Audio Precision System Two Cascade or Cascade Plus test system.
(2) f_{SMIN} = min (f_{SIN}, f_{SOUT}).
(3) f_{SMAX} = max (f_{SIN}, f_{SOUT}).
(4) Power-supply current for power-down modes is measured without loading.
(5) Dynamic current is measured with active loading and the excercized output pins equal to ±2mA.

ELECTRICAL CHARACTERISTICS (continued)

All specifications at T_A = +25°C, VDD33 = +3.3V, V_{IO} = +3.3V, REGEN = High, and VDD18 floating, unless otherwise noted.

PARAMETER		CONDITIONS	SRC4184 MIN	TYP	MAX	UNITS
DIGITAL ATTENUATION		Software Mode Only				
Minimum				0		dB
Maximum				−127.5		dB
Step Size				0.5		dB
Mute Attenuation		24-Bit Word Length		−128		dB
DIGITAL INTERPOLATION FILTER CHARACTERISTICS						
Passband					$0.4535 \times f_{SIN}$	Hz
Passband Ripple					±0.007	dB
Transition Band			$0.4535 \times f_{SIN}$		$0.5465 \times f_{SIN}$	Hz
Stop Band			$0.5465 \times f_{SIN}$			Hz
Stop Band Attenuation			−128			dB
Group Delay (64 sample buffer)		Decimation Filter Enabled		$102.53125/f_{SIN}$		seconds
Group Delay (64 sample buffer)		Direct Downsampling Enabled		$102/f_{SIN}$		seconds
Group Delay (32 sample buffer)		Decimation Filter Enabled		$70.53125/f_{SIN}$		seconds
Group Delay (32 sample buffer)		Direct Downsampling Enabled		$70/f_{SIN}$		seconds
Group Delay (16 sample buffer)		Decimation Filter Enabled		$54.53125/f_{SIN}$		seconds
Group Delay (16 sample buffer)		Direct Downsampling Enabled		$54/f_{SIN}$		seconds
Group Delay (8 sample buffer)		Decimation Filter Enabled		$46.53125/f_{SIN}$		seconds
Group Delay (8 sample buffer)		Direct Downsampling Enabled		$46/f_{SIN}$		seconds
DIGITAL DECIMATION FILTER CHARACTERISTICS						
Passband					$0.4535 \times f_{SOUT}$	Hz
Passband Ripple					±0.008	dB
Transition Band			$0.4535 \times f_{SOUT}$		$0.5465 \times f_{SOUT}$	Hz
Stop Band			$0.5465 \times f_{SOUT}$			Hz
Stop Band Attenuation			−128			dB
Group Delay						
Decimation Filter		Decimation Filter Enabled		$36.46875/f_{SOUT}$		seconds
Direct Downsampling		Direct Downsampling Enabled		0		seconds
DIGITAL DE-EMPHASIS						
De-Emphasis Error for f_S = 32kHz, 44.1kHz, or 48kHz		De-Emphasis Enabled		0.001		dB
DIGITAL I/O CHARACTERISTICS						
High-Level Input Voltage	V_{IH}		$0.7 \times V_{IO}$		V_{IO}	V
Low-Level Input Voltage	V_{IL}		0		$0.3 \times V_{IO}$	V
High-Level Input Current	I_{IH}			0.5	10	μA
Low-Level Input Current	I_{IL}			0.5	10	μA
High-Level Output Voltage	V_{OH}	I_O = −4mA	$0.8 \times V_{IO}$		V_{IO}	V
Low-Level Output Voltage	V_{OL}	I_O = +4mA	0		$0.2 \times V_{IO}$	V
Input Capacitance	C_{IN}			3		pF
SWITCHING CHARACTERISTICS						
Reference Clock Timing						
RCKI Frequency(2)(3)			$128 \times f_{SMIN}$		50	MHz
RCKI Period	t_{RCKIP}		20		$1/(128 \times f_{SMIN})$	ns
RCKI Pulsewidth High	t_{RCKIH}		$0.4 \times t_{RCKIP}$			ns
RCKI Pulsewidth Low	t_{RCKIL}		$0.4 \times t_{RCKIP}$			ns
Reset Timing						
$\overline{RST}$ Pulsewidth Low	t_{RSTL}		500			ns
Delay Following $\overline{RST}$ Rising Edge		Software Mode Only	500			μs
Input Serial Port Timing						
LRCKI to BCKI Setup Time	t_{LRIS}		10			ns
BCKI Pulsewidth High	t_{SIH}		10			ns
BCKI Pulsewidth Low	t_{SIL}		10			ns
SDIN Data Setup Time	t_{LDIS}		10			ns
SDIN Data Hold Time	t_{LDIH}		10			ns

(1) Dynamic performance is measured with an Audio Precision System Two Cascade or Cascade Plus test system.
(2) f_{SMIN} = min (f_{SIN}, f_{SOUT}).
(3) f_{SMAX} = max (f_{SIN}, f_{SOUT}).
(4) Power-supply current for power-down modes is measured without loading.
(5) Dynamic current is measured with active loading and the excercized output pins equal to ±2mA.

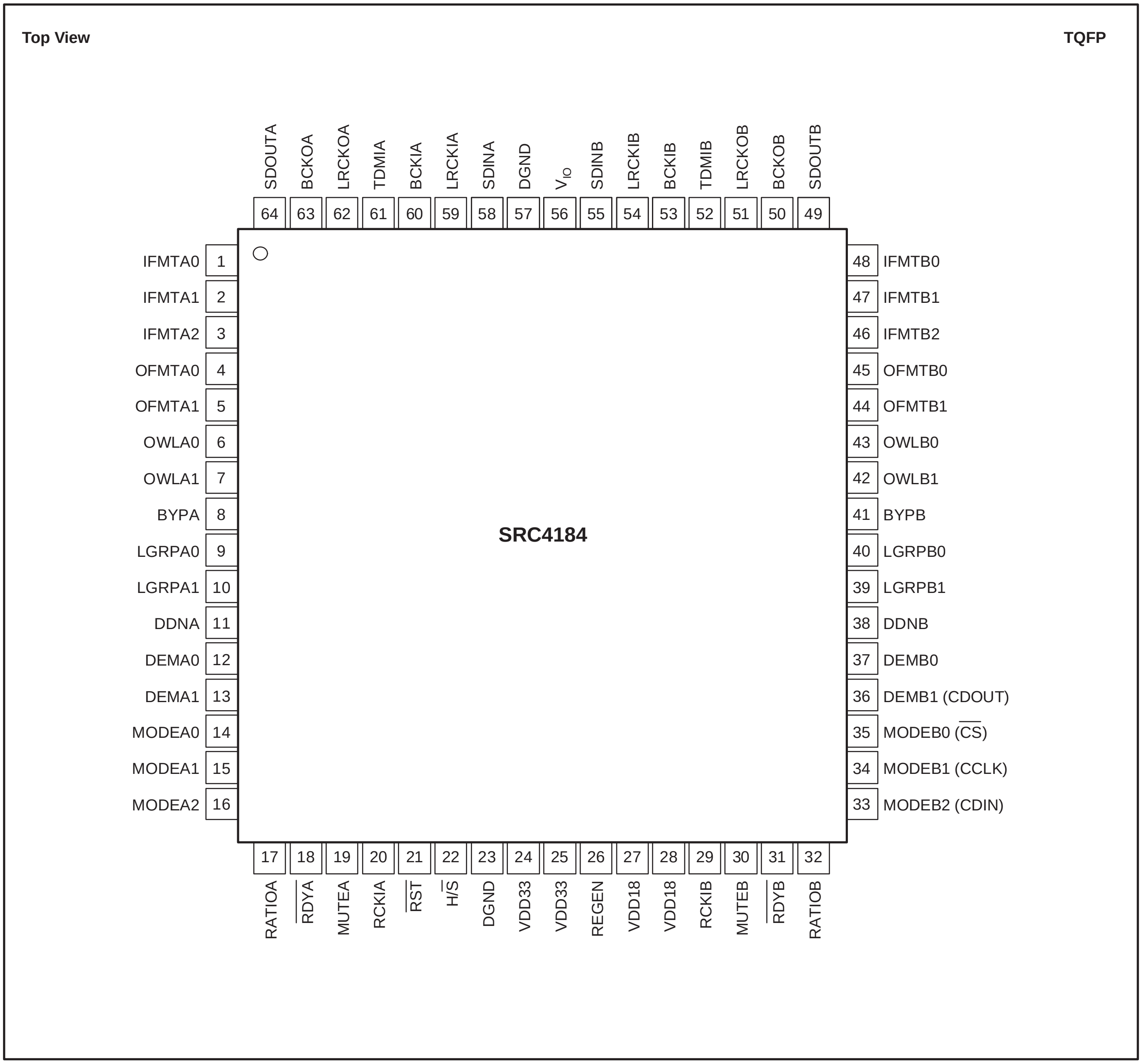
ELECTRICAL CHARACTERISTICS (continued)

All specifications at T_A = +25°C, VDD33 = +3.3V, V_{IO} = +3.3V, REGEN = High, and VDD18 floating, unless otherwise noted.

PARAMETER		CONDITIONS	SRC4184 MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS (continued)						
Output Serial Port Timing						
SDOUT Data Delay Time	t_{DOPD}				10	ns
SDOUT Data Hold Time	t_{DOH}		2			ns
BCKO Pulsewidth High	t_{SOH}		10			ns
BCKO Pulsewidth Low	t_{SOL}		5			ns
TDM Mode Timing						
LRCKO Setup Time	t_{LROS}		10			ns
LRCKO Hold Time	t_{LROH}		10			ns
TDMI Data Setup Time	t_{TDMS}		10			ns
TDMI Data Hold Time	t_{TDMH}		10			ns
SPI Timing						
CCLK Frequency					25	MHz
CDATA Setup Time	t_{CDS}		12			ns
CDATA Hold Time	t_{CDH}		8			ns
$\overline{CS}$ Falling to CCLK Rising	t_{CSCR}		15			ns
CCLK Falling to $\overline{CS}$ Rising	t_{CFCS}		12			ns
CCLK Falling to CDOUT Data Valid	t_{CFDO}				5	ns
$\overline{CS}$ Rising to CDOUT High Impedance	t_{CSZ}				5	ns
POWER SUPPLIES(4, 5)						
Operating Voltage						
VDD18		REGEN = 0	+1.65	+1.8	+2.0	V
VDD33		REGEN = 1	+3.0	+3.3	+3.6	V
V_{IO}			+1.65	+3.3	+3.6	V
Supply Current		VDD18 = +1.8V, V_{IO} = +1.8V, REGEN = 0				
IDD, Hard Power-Down		$\overline{RST}$ = 0, No Clocks			100	µA
IDD, Soft Power-Down		$\overline{PDN}$ Bit = 0, No Clocks		100		µA
IDD, Dynamic		f_{SIN} = 96kHz, f_{SOUT} = 192kHz		80		mA
IIO, Hard Power-Down		$\overline{RST}$ = 0, No Clocks			100	µA
IIO, Soft Power-Down		$\overline{PDN}$ Bit = 0, No Clocks		100		µA
IIO, Dynamic		f_{SIN} = 96kHz, f_{SOUT} = 192kHz		6		mA
Total Power Dissipation		VDD18 = +1.8V, V_{IO} = +1.8V, REGEN = 0				
P_D, Hard Power-Down		$\overline{RST}$ = 0, No Clocks			1	mW
P_D, Soft Power-Down		$\overline{PDN}$ Bit = 0, No Clocks		360		µW
P_D, Dynamic		f_{SIN} = f_{SOUT} = 192kHz		155		mW
Supply Current		VDD33 = +3.3V, V_{IO} = +3.3V, REGEN = 1				
IDD, Hard Power-Down		$\overline{RST}$ = 0, No Clocks			100	µA
IDD, Soft Power-Down		$\overline{PDN}$ Bit = 0, No Clocks		6		mA
IDD, Dynamic		f_{SIN} = 96kHz, f_{SOUT} = 192kHz		90		mA
IIO, Hard Power-Down		$\overline{RST}$ = 0, No Clocks			100	µA
IIO, Soft Power-Down		$\overline{PDN}$ Bit = 0, No Clocks		100		µA
IIO, Dynamic		f_{SIN} = 96kHz, f_{SOUT} = 192kHz		6		mA
Total Power Dissipation		VDD33 = +3.3V, V_{IO} = +3.3V, REGEN = 1				
P_D, Hard Power-Down		$\overline{RST}$ = 0, No Clocks			1	mW
P_D, Soft Power-Down		$\overline{PDN}$ Bit = 0, No Clocks		21		mW
P_D, Dynamic		f_{SIN} = f_{SOUT} = 192kHz		320		mW

(1) Dynamic performance is measured with an Audio Precision System Two Cascade or Cascade Plus test system.
(2) f_{SMIN} = min (f_{SIN}, f_{SOUT}).
(3) f_{SMAX} = max (f_{SIN}, f_{SOUT}).
(4) Power-supply current for power-down modes is measured without loading.
(5) Dynamic current is measured with active loading and the excercized output pins equal to ±2mA.

PIN CONFIGURATION



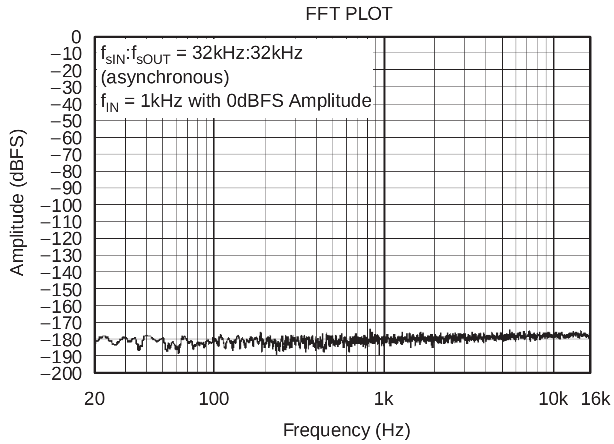
PIN DESCRIPTIONS

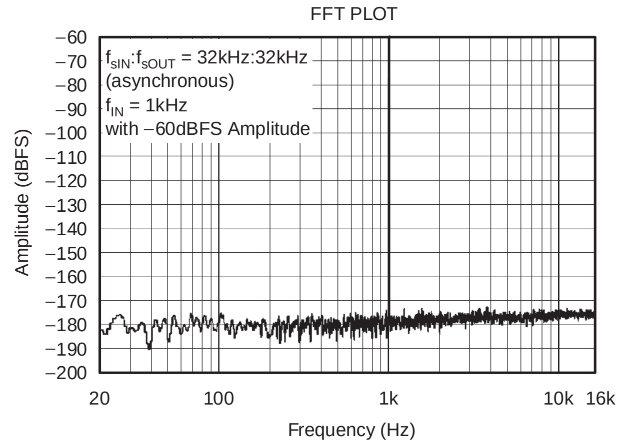
PIN #	NAME	I/O	DESCRIPTION
1	IFMTA0	Input	SRC A Audio Input Data Format(1)
2	IFMTA1	Input	SRC A Audio Input Data Format(1)
3	IFMTA2	Input	SRC A Audio Input Data Format(1)
4	OFMTA0	Input	SRC A Audio Output Data Format(1)
5	OFMTA1	Input	SRC A Audio Output Data Format(1)
6	OWLA0	Input	SRC A Audio Output Data Word Length(1)
7	OWLA1	Input	SRC A Audio Output Data Word Length(1)
8	BYPA	Input	SRC A Bypass Mode (Active High)
9	LGRPA0	Input	SRC A Low Group Delay Mode(1)
10	LGRPA1	Input	SRC A Low Group Delay Mode(1)
11	DDNA	Input	SRC A Direct Downsampling Mode (Active High)(1)
12	DEMA0	Input	SRC A Digital De-Emphasis Filter Mode(1)
13	DEMA1	Input	SRC A Digital De-Emphasis Filter Mode(1)
14	MODEA0	Input	SRC A Serial Port Mode(1)
15	MODEA1	Input	SRC A Serial Port Mode(1)
16	MODEA2	Input	SRC A Serial Port Mode(1)
17	RATIOA	Output	SRC A Ratio Flag
18	$\overline{\text{RDYA}}$	Output	SRC A Ready Flag (Active Low)
19	MUTEA	Input	SRC A Output Soft Mute
20	RCKIA	Input	SRC A Reference Clock
21	$\overline{\text{RST}}$	Input	Reset and Power-Down (Active Low)
22	H/$\overline{\text{S}}$	Input	Control Mode (0 = Software, 1 = Hardware)
23	DGND	Ground	Digital Ground
24, 25	VDD33	Power	Core Supply, +3.3V. Required when REGEN is high. When REGEN is low, VDD33 must be left unconnected.
26	REGEN	Input	Voltage Regulator Enable (Active High)
27, 28	VDD18	Power	Core Supply, +1.8V. Required when REGEN is low. When REGEN is high, VDD18 must be left unconnected.
29	RCKIB	Input	SRC B Reference Clock
30	MUTEB	Input	SRC B Output Soft Mute
31	$\overline{\text{RDYB}}$	Output	SRC B Ready Flag (Active Low)
32	RATIOB	Output	SRC B Ratio Flag
33	MODEB2 or CDIN	Input	SRC B Serial Port Mode(1) or SPI Port Serial Data Input(2)
34	MODEB1 or CCLK	Input	SRC B Serial Port Mode(1) or SPI Port Data Clock(2)
35	MODEB0 or $\overline{\text{CS}}$	Input	SRC B Serial Port Mode(1) or SPI Port Chip Select (Active Low)(2)
36	DEMB1 or CDOUT	I/O	SRC B Digital De-Emphasis Filter Mode(1) or SPI Port Serial Data Output(2)
37	DEMB0	Input	SRC B Digital De-Emphasis Filter Mode(1)
38	DDNB	Input	SRC B Direct Downsampling Mode (Active High)(1)
39	LGRPB1	Input	SRC B Low Group Delay Mode(1)
40	LGRPB0	Input	SRC B Low Group Delay Mode(1)
41	BYPB	Input	SRC B Bypass Mode (Active High)
42	OWLB1	Input	SRC B Audio Output Data Word Length(1)
43	OWLB0	Input	SRC B Audio Output Data Word Length(1)
44	OFMTB1	Input	SRC B Audio Output Data Format(1)
45	OFMTB0	Input	SRC B Audio Output Data Format(1)
46	IFMTB2	Input	SRC B Audio Input Data Format(1)
47	IFMTB1	Input	SRC B Audio Input Data Format(1)
48	IFMTB0	Input	SRC B Audio Input Data Format(1)
49	SDOUTB	Output	SRC B Audio Output Data
50	BCKOB	I/O	SRC B Audio Output Bit Clock
51	LRCKOB	I/O	SRC B Audio Output Left/Right or Word Clock
52	TDMIB	Input	SRC B TDM Input Data (TDM Format Only)
53	BCKIB	I/O	SRC B Audio Input Bit Clock
54	LRCKIB	I/O	SRC B Audio Input Left/Right or Word Clock
55	SDINB	Input	SRC B Audio Input Data
56	V_{IO}	Power	Digital I/O Supply, +1.65V to +3.6V
57	DGND	Ground	Digital Ground
58	SDINA	Input	SRC A Audio Input Data
59	LRCKIA	I/O	SRC A Audio Input Left/Right or Word Clock
60	BCKIA	I/O	SRC A Audio Input Bit Clock
61	TDMIA	Input	SRC A TDM Input Data (TDM Format Only)
62	LRCKOA	I/O	SRC A Audio Output Left/Right or Word Clock
63	BCKOA	I/O	SRC A Audio Output Bit Clock
64	SDOUTA	Output	SRC A Audio Output Data

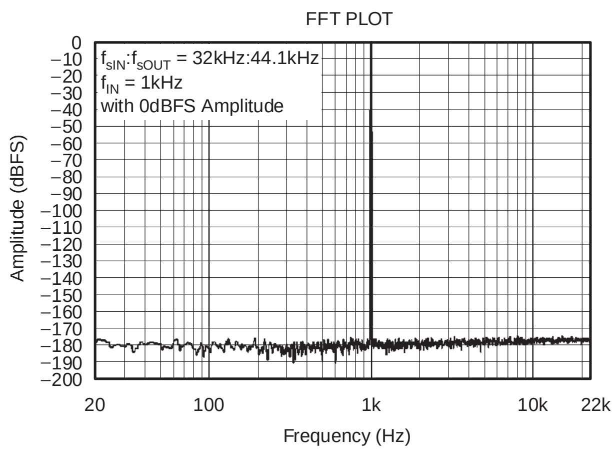
(1) Disabled in Software control mode.
(2) Disabled in Hardware control mode.

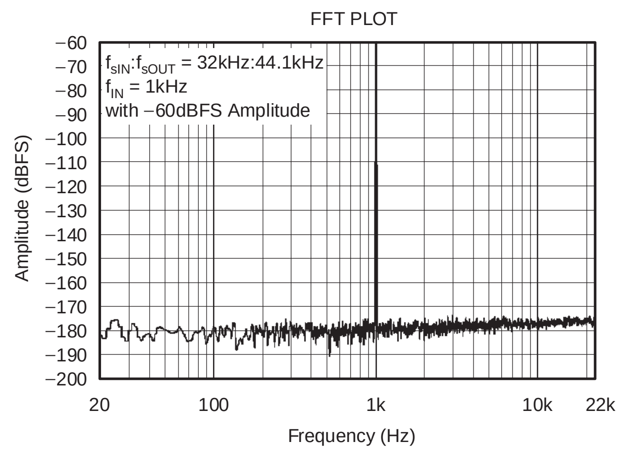
TYPICAL CHARACTERISTICS

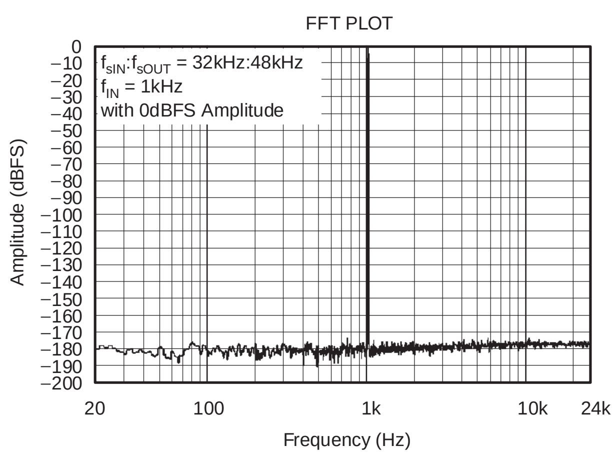
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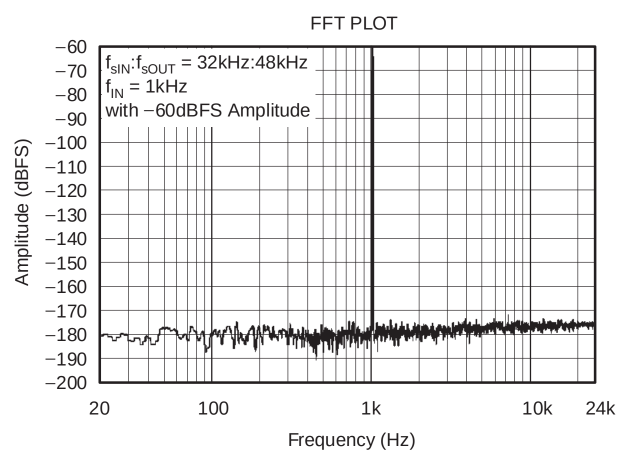






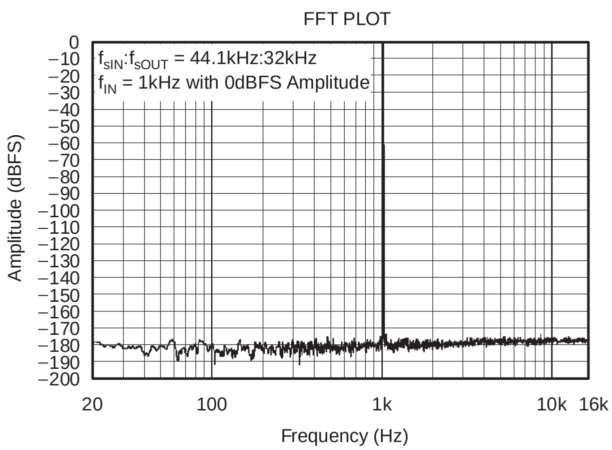


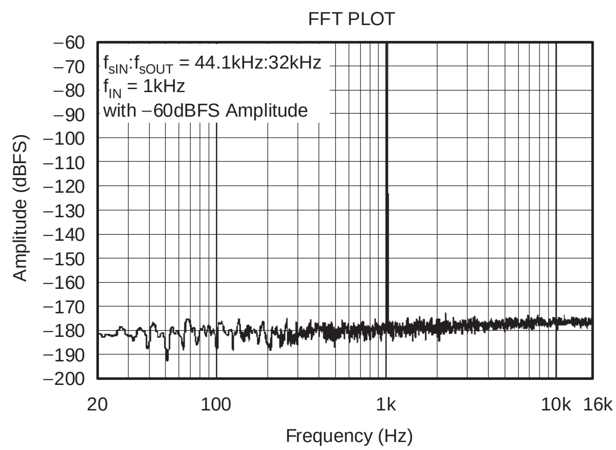


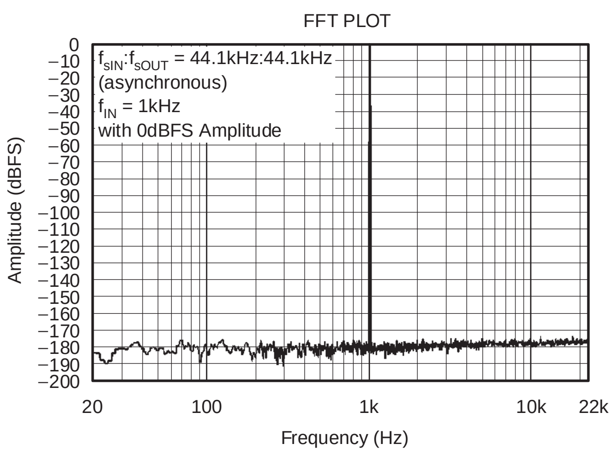


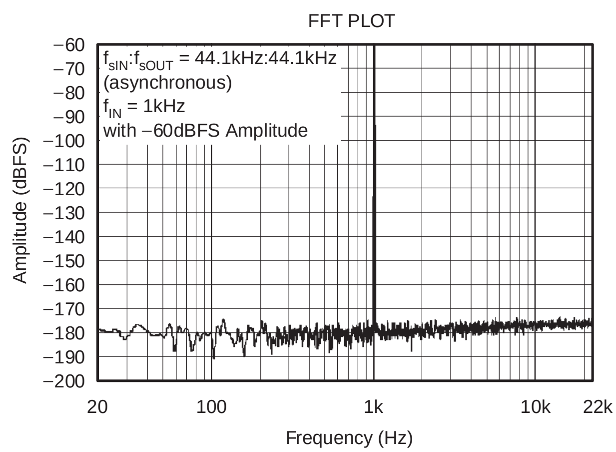
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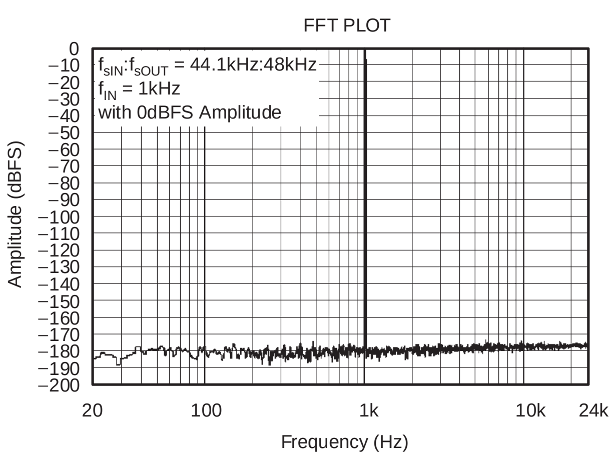
All specifications at T_A = +25°C, VDD33 = +3.3V, V_{IO} = +3.3V, REGEN = High, and VDD18 floating, unless otherwise noted.

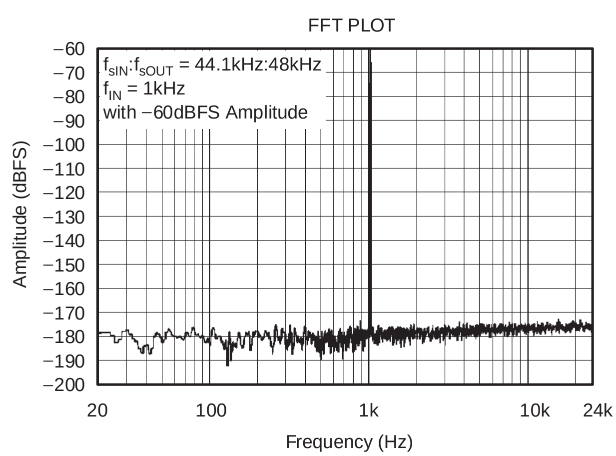






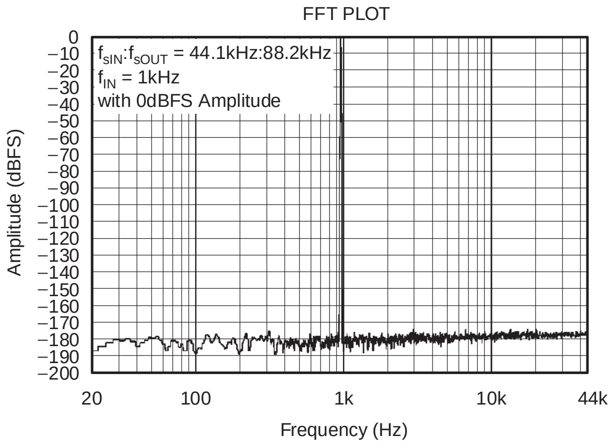


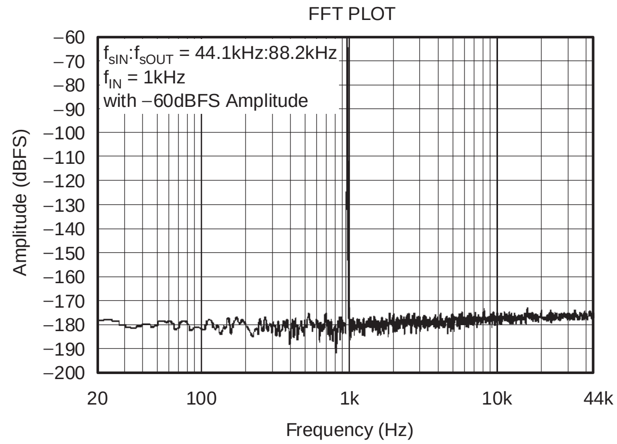


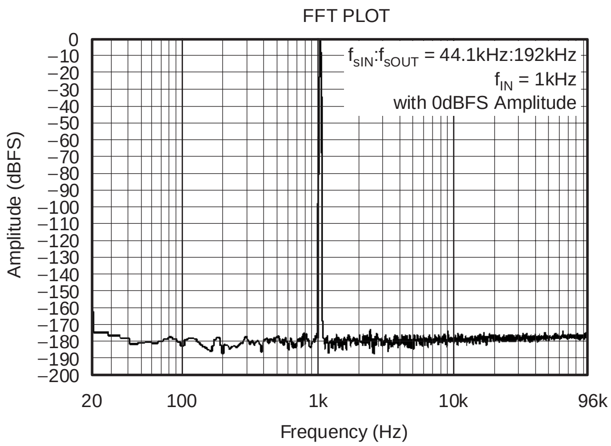


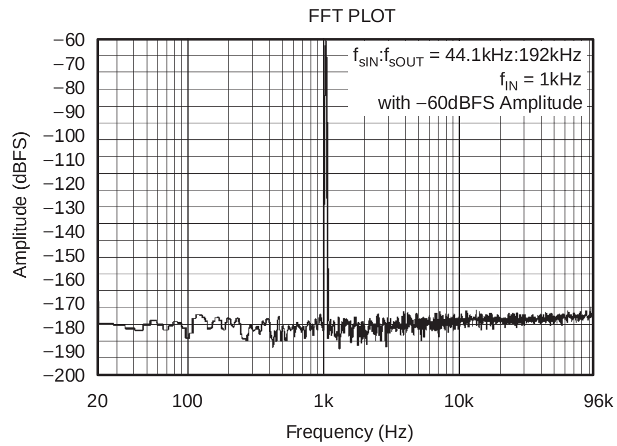
TYPICAL CHARACTERISTICS (continued)

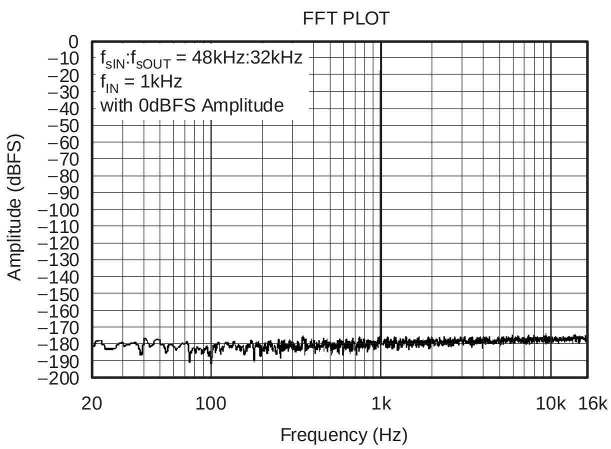
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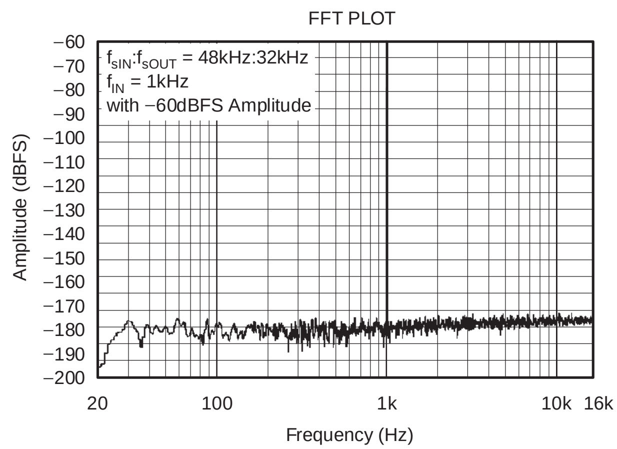






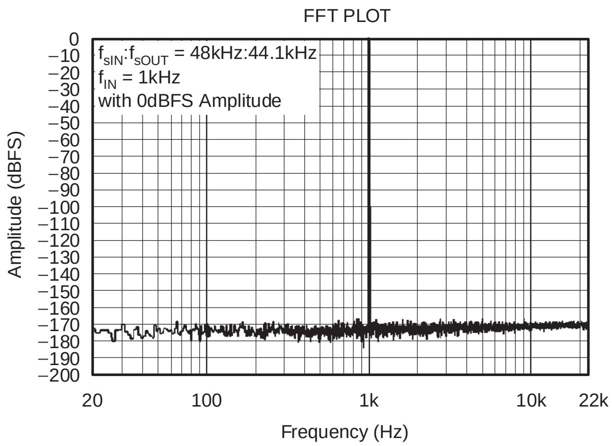


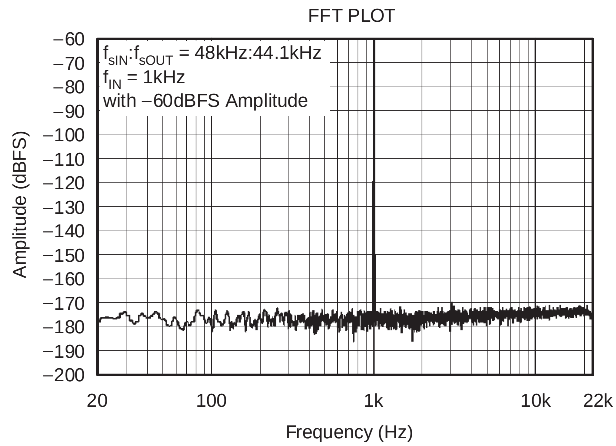


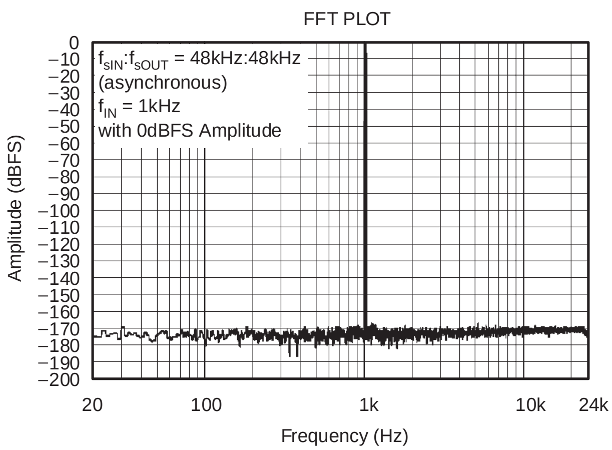


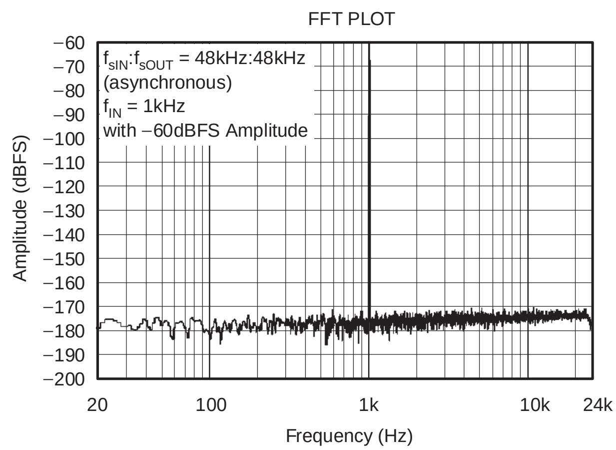
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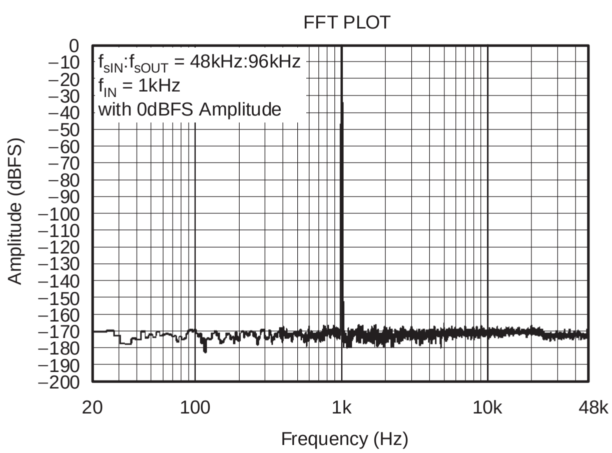
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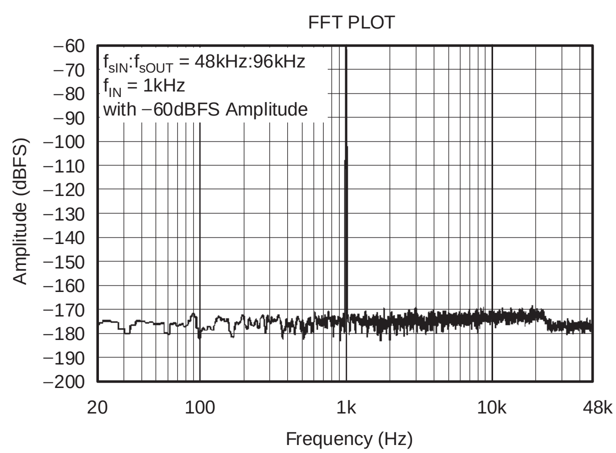






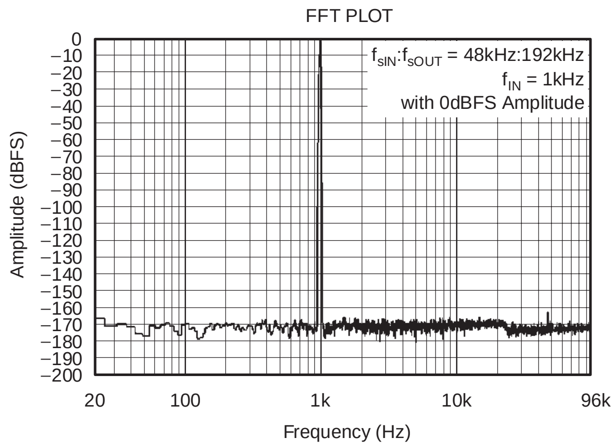


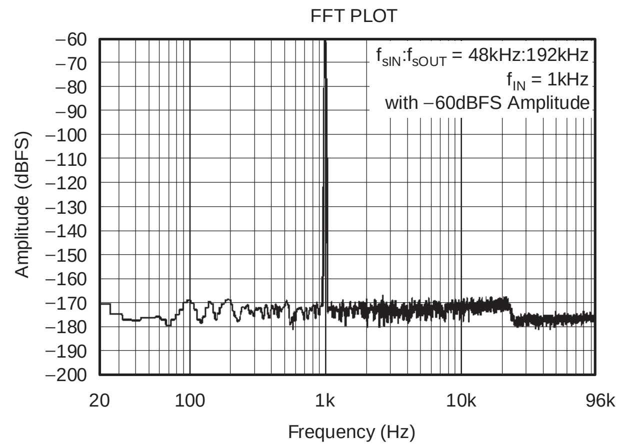


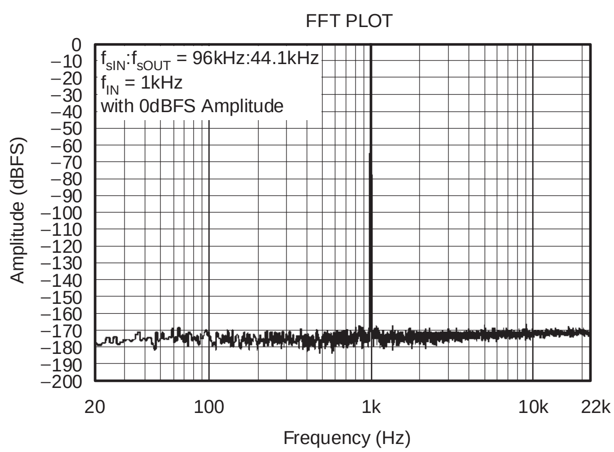


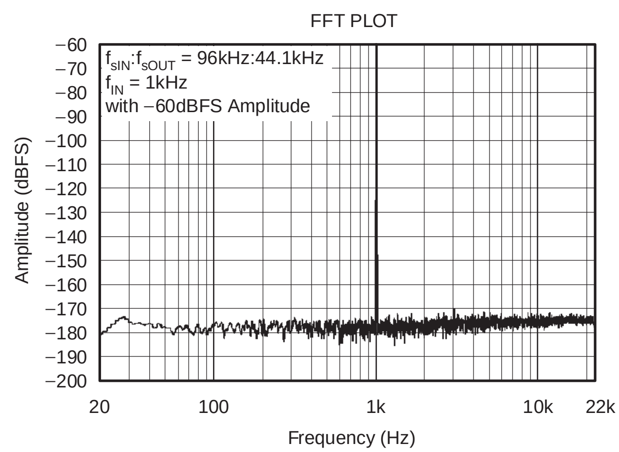
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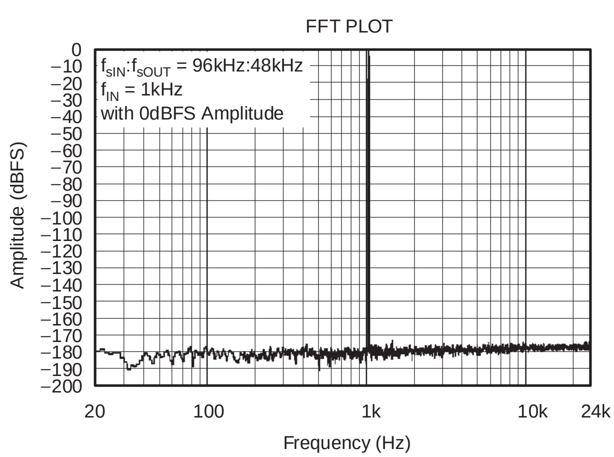
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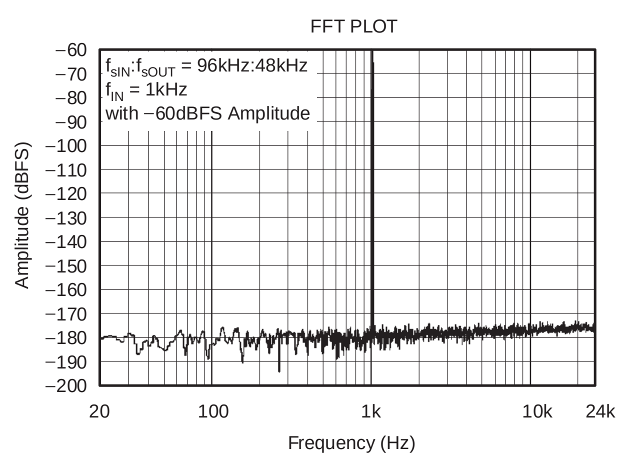






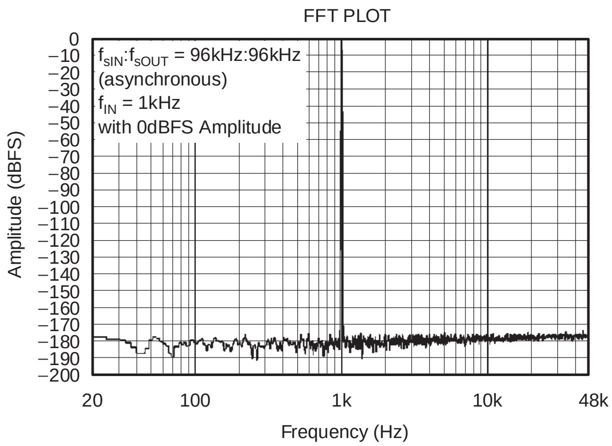


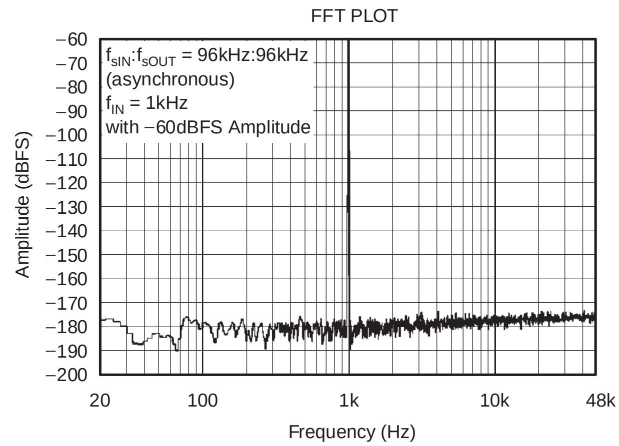


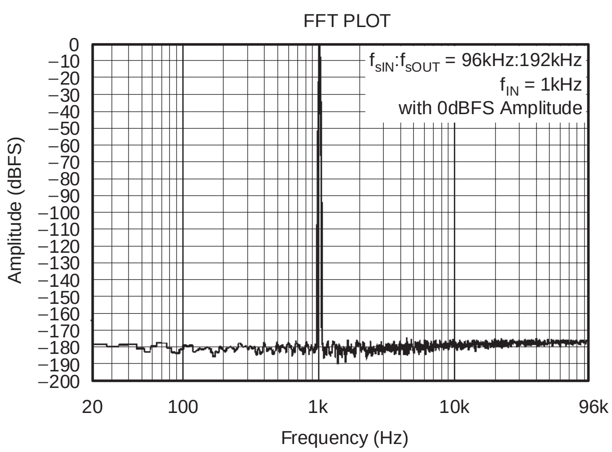


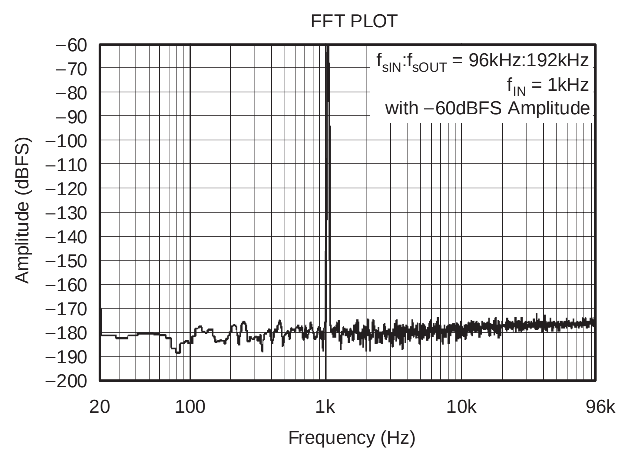
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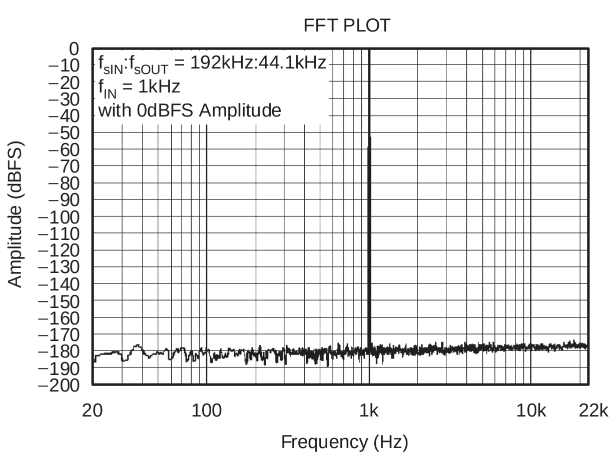
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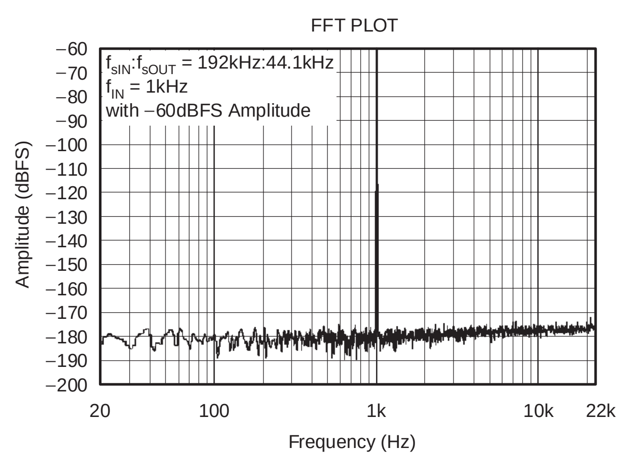






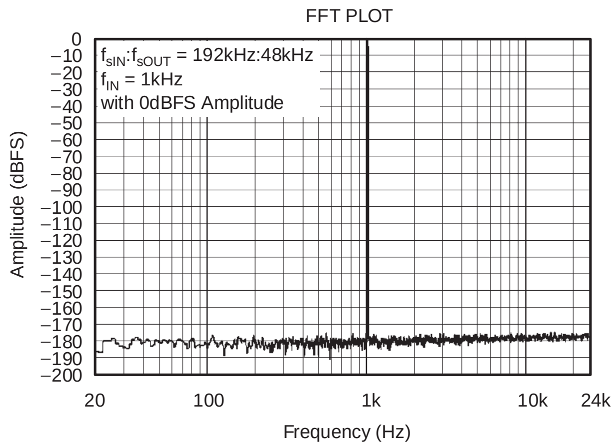


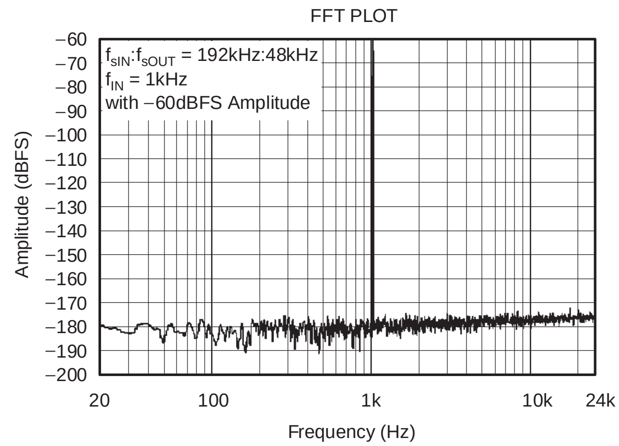


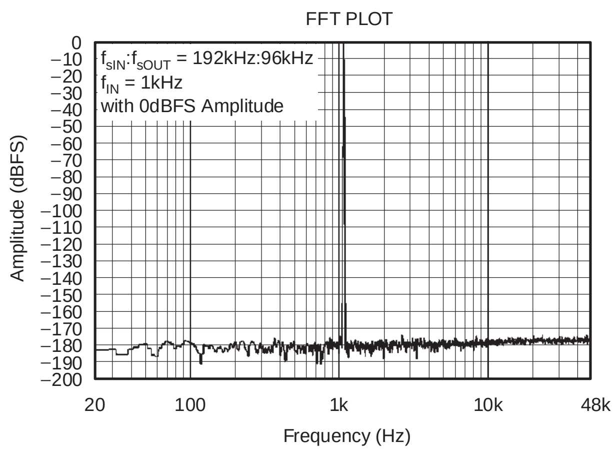


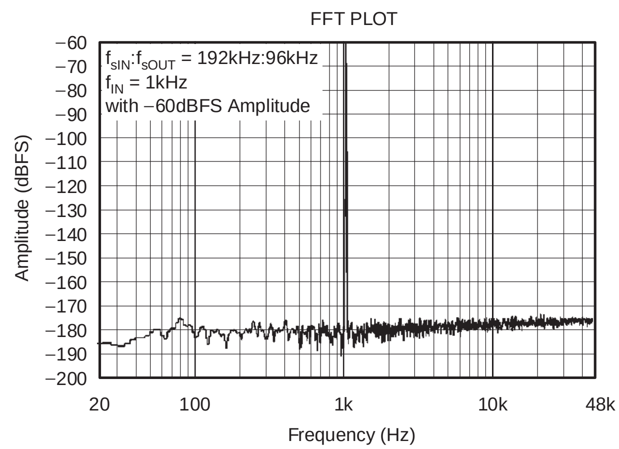
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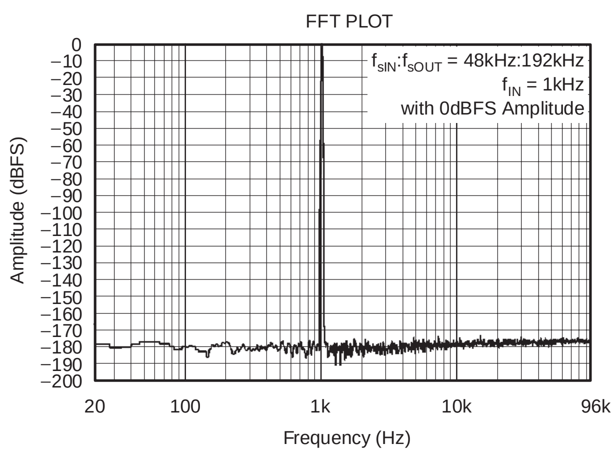
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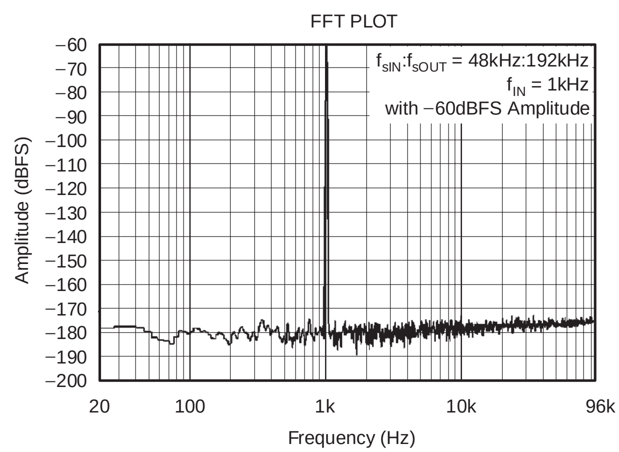






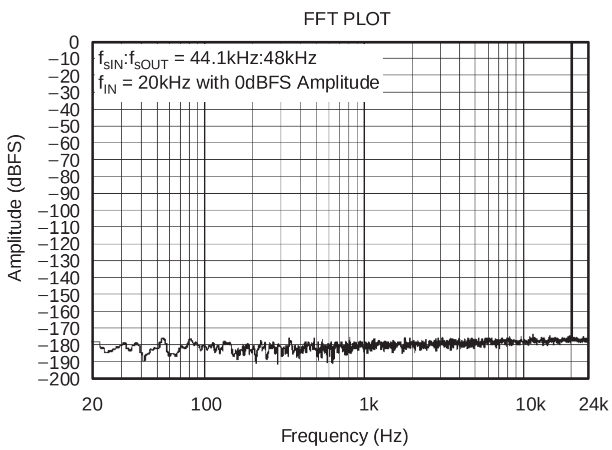


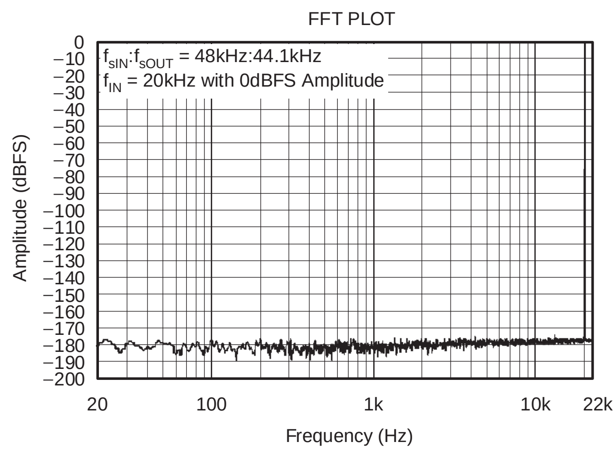


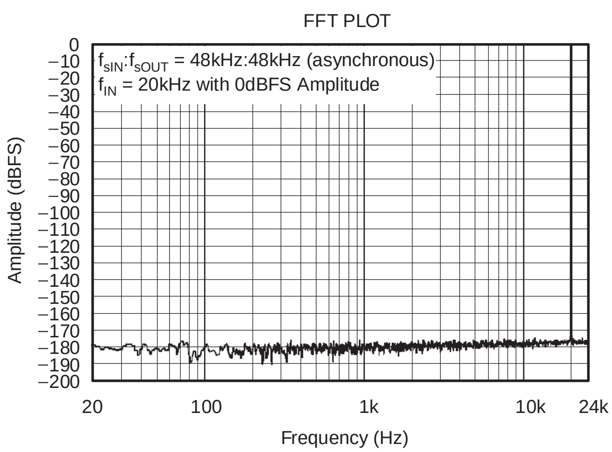


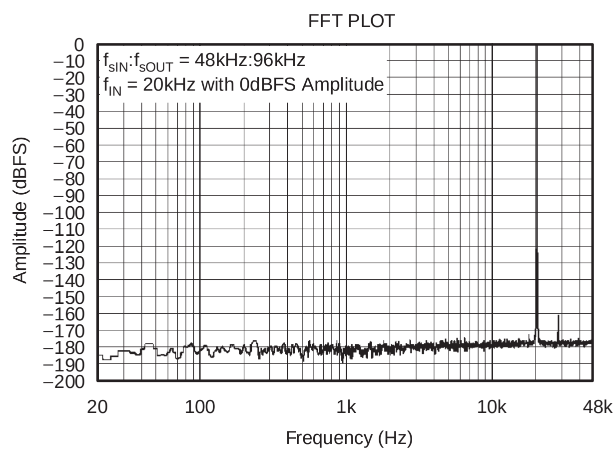
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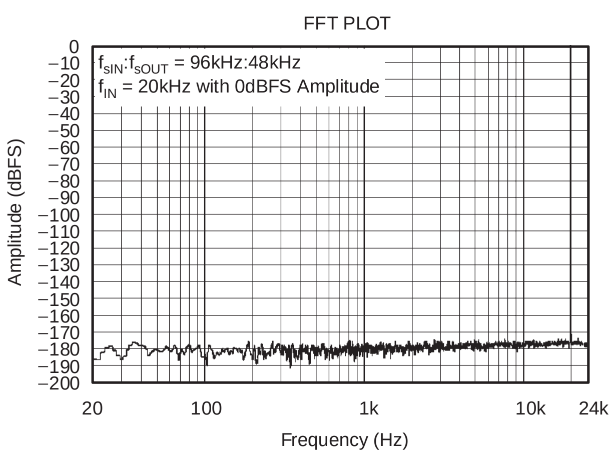
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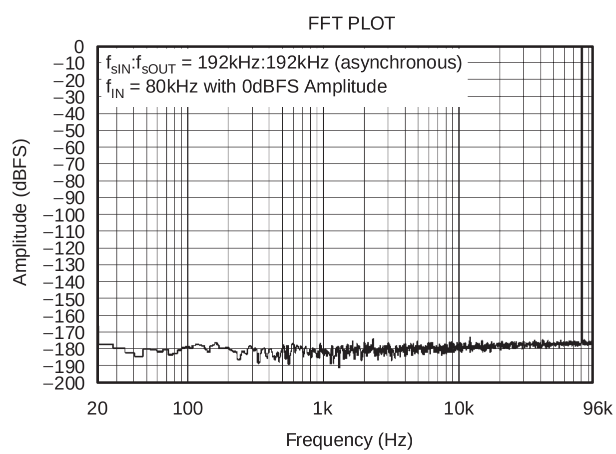








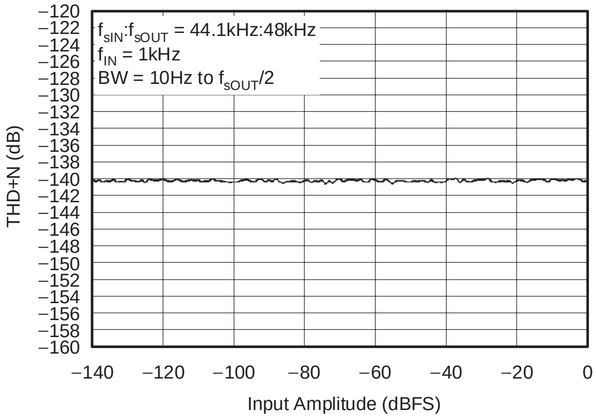




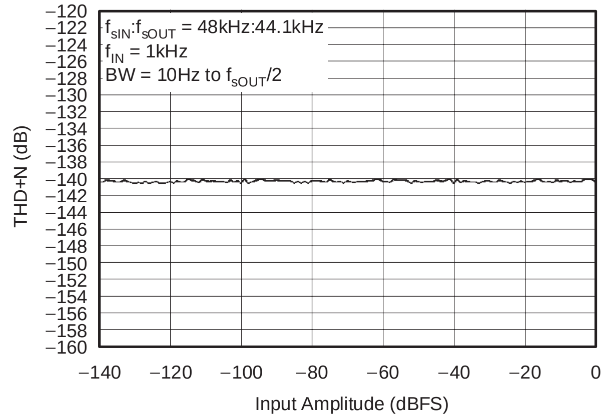
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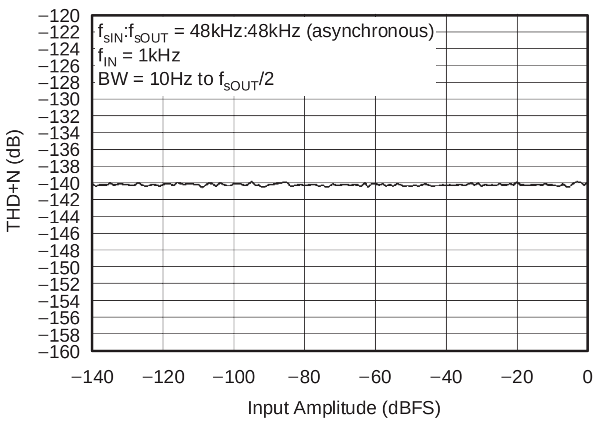
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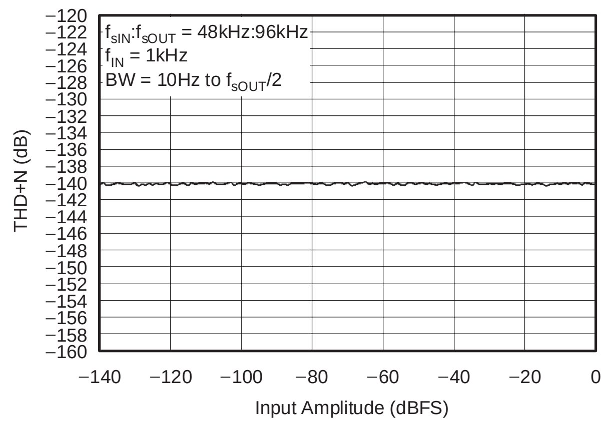
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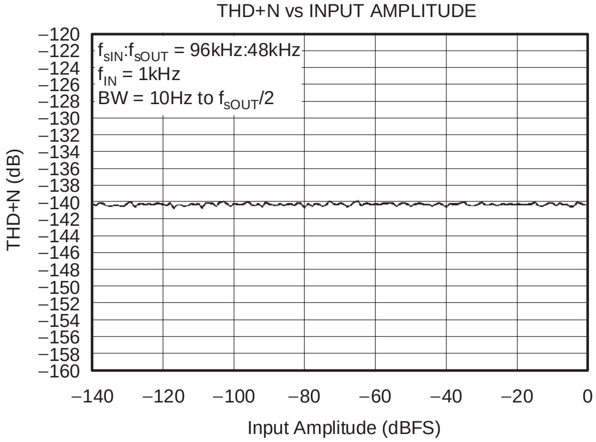
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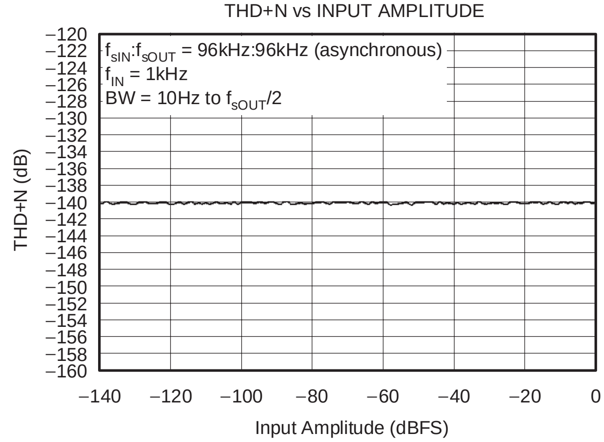
THD+N vs INPUT AMPLITUDE



THD+N vs INPUT AMPLITUDE

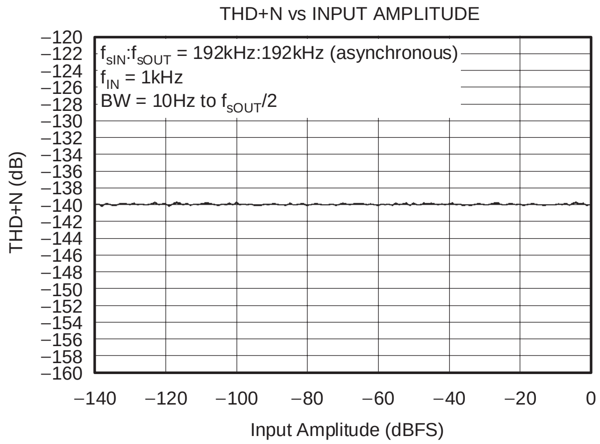


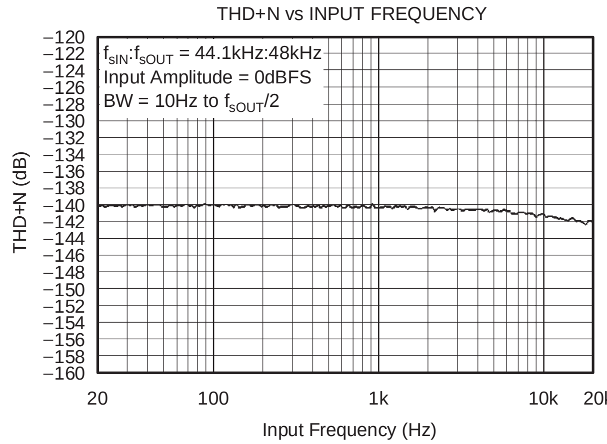
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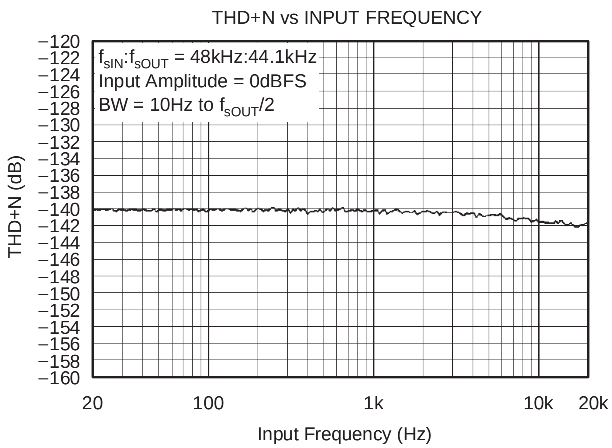


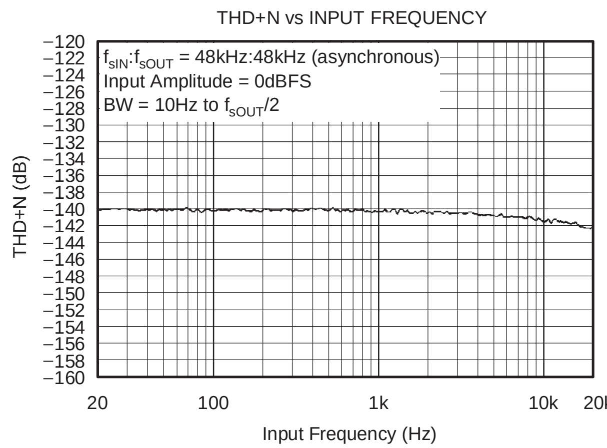
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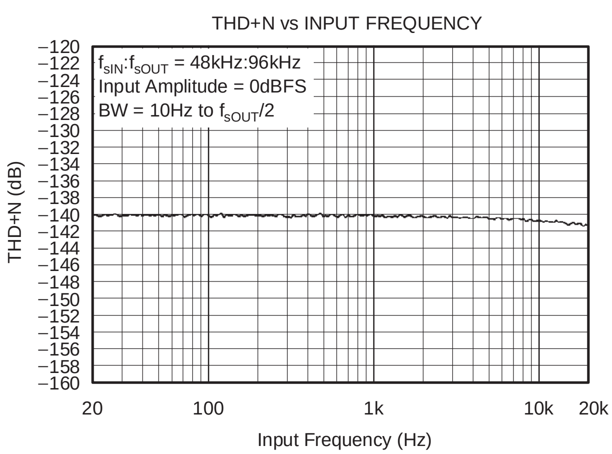
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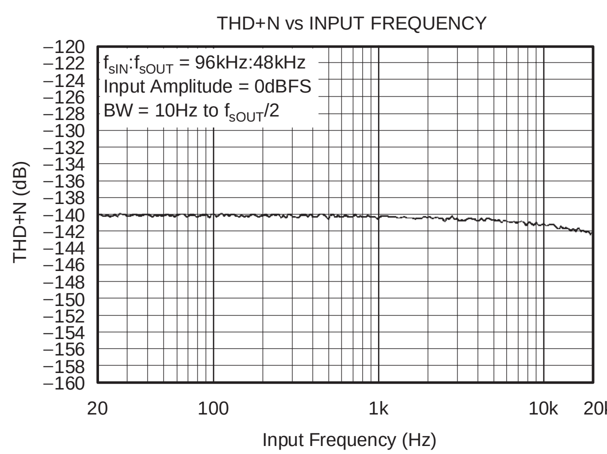






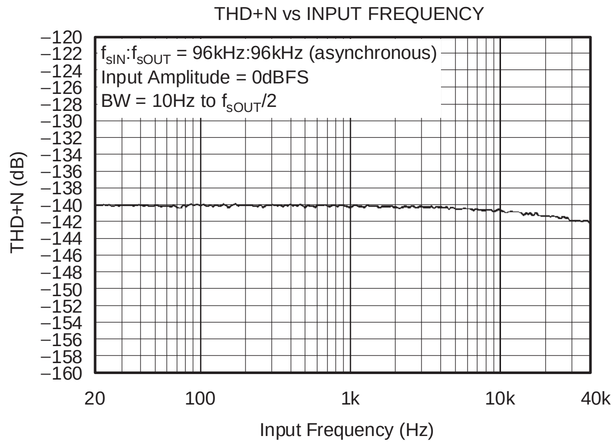


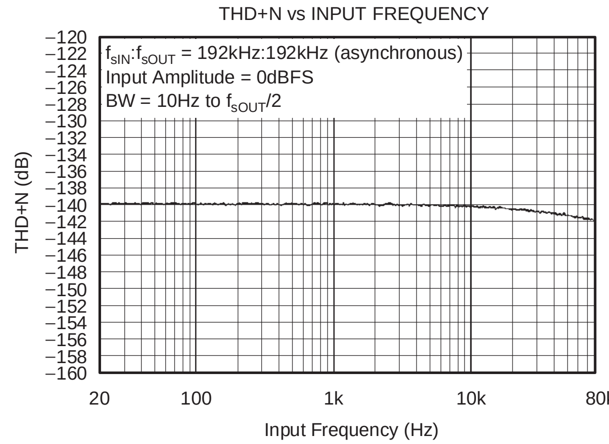


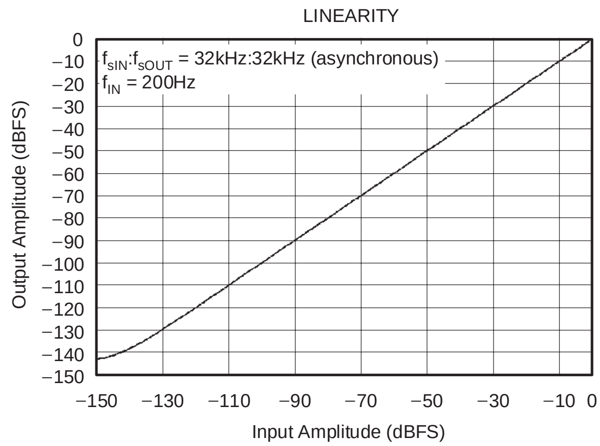


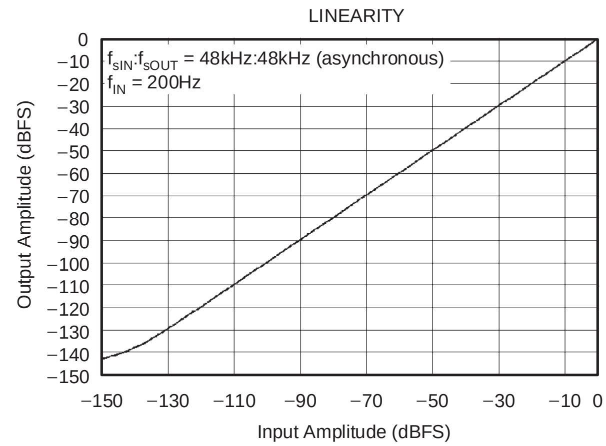
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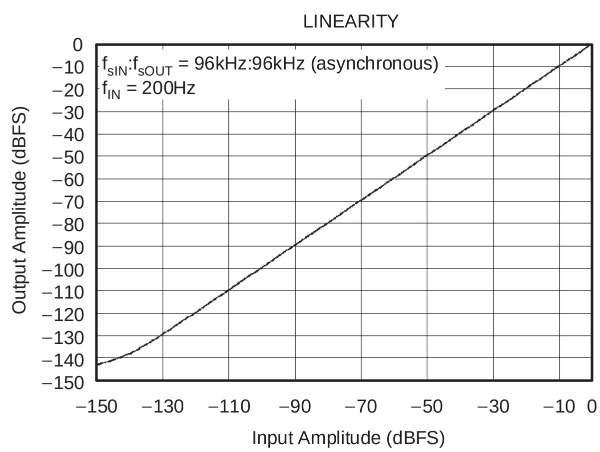
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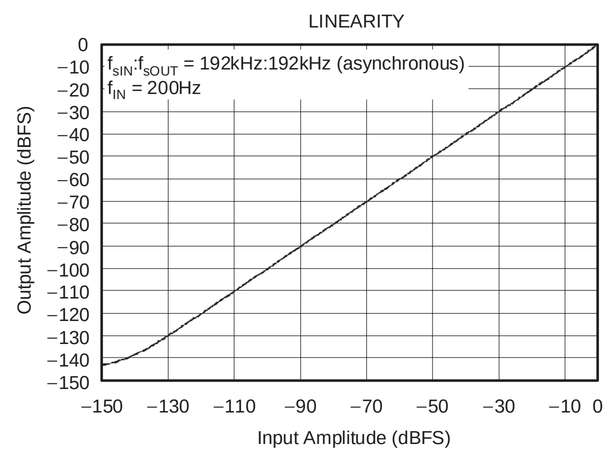






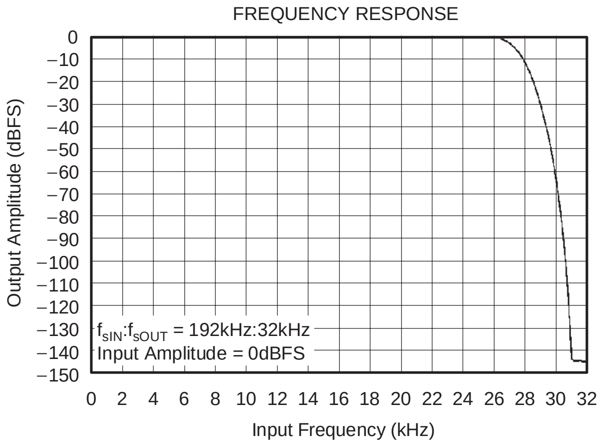


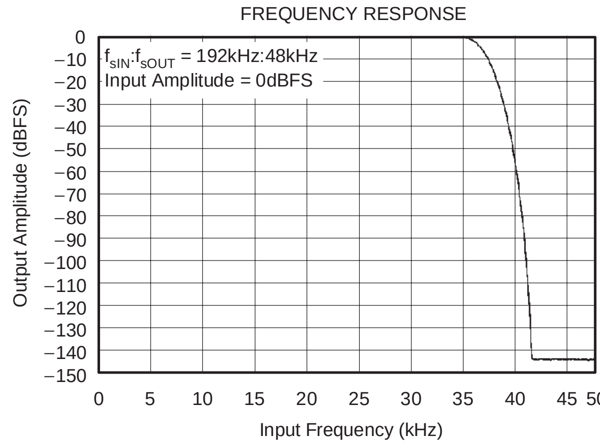


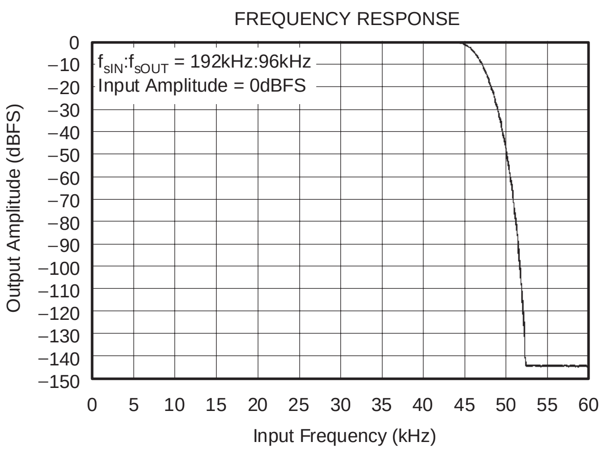


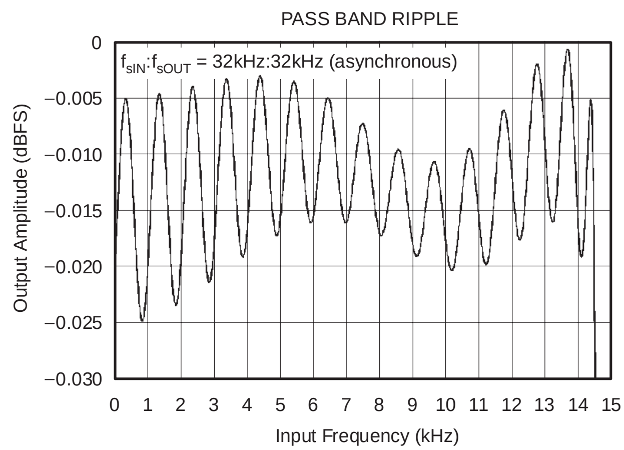
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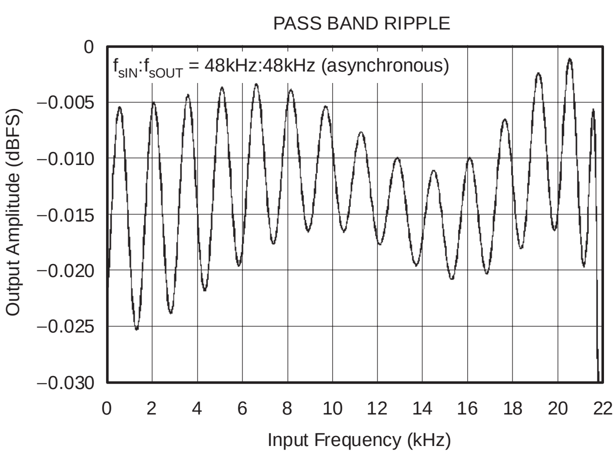
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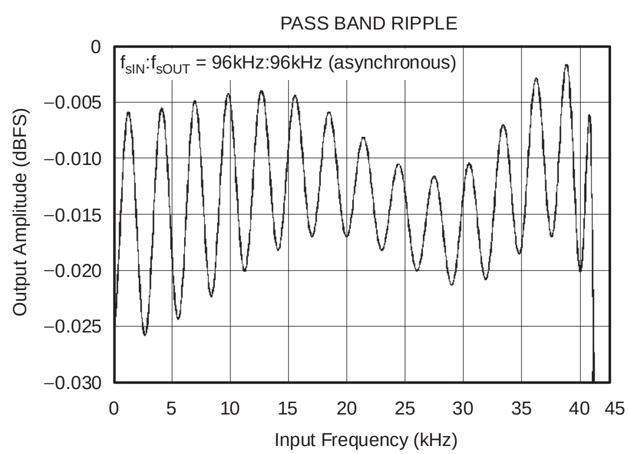






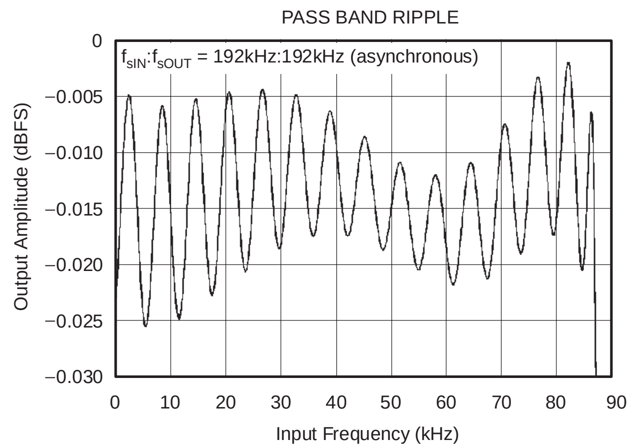






TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = +25°C, VDD33 = +3.3V, V_{IO} = +3.3V, REGEN = High, and VDD18 floating, unless otherwise noted.



PRODUCT OVERVIEW

The SRC4184 is a four-channel, asynchronous sample rate converter (ASRC), implemented as two stereo sections, referred to as SRC A and SRC B. Operation at input and output sampling frequencies up to 212kHz is supported, with a continuous input/output sampling ratio range of 16:1 to 1:16. Excellent dynamic range and THD+N are achieved by employing high-performance, linear-phase digital filtering with better than 128dB of image rejection. The digital filters provide settings for lower latency processing, including low group delay options for the interpolation filter and a direct downsampling option for the decimation filter. Digital de-emphasis filtering is included, supporting 32kHz, 44.1kHz, and 48kHz sampling frequencies.

The audio input and output ports support standard audio data formats, as well as a time division multiplexed (TDM) format. Word lengths of 24-, 20-, 18-, and 16-bits are supported. Input and output ports may operate in Slave mode, deriving their word and bit clocks from external input and output devices. Alternatively, one port may operate in Master mode while the other remains in Slave mode. In Master mode, the LRCK and BCK clocks are derived from the reference clock inputs, either RCKIA or RCKIB. The flexible configuration options for the input and output ports allow connections to a variety of audio data converters, digital audio interface devices, and digital signal processors.

A bypass mode is included, which allows audio data to be passed directly from the input port to the output port, bypassing the ASRC function. The bypass option is useful for passing through compressed or encoded audio data, as well as non-audio data (that is, control or status information).

A soft mute function is available for the SRC4184 in both Hardware and Software modes. Digital output attenuation is available only in Software mode. Both soft mute and digital attenuation functions provide artifact-free operation. The mute attenuation is typically −128dB, while the digital attenuation function is adjustable from 0dB to −127.5dB in 0.5dB steps.

The SRC4184 includes a four-wire SPI port, which is used to access on-chip control and status registers in Software mode. The SPI port facilitates interfacing to microprocessors or digital signal processors that support synchronous serial peripherals. In Hardware mode, dedicated control pins are provided for the majority of the SRC4184 functions. These pins can be hard-wired or driven by logic or host control.

FUNCTIONAL BLOCK DIAGRAM

Figure 1 shows a functional block diagram of the SRC4184. The SRC4184 is segmented into two stereo SRC sections, referred to as SRC A and SRC B. Each section can operate independently from the other. Each section has individual sets of configuration pins in Hardware mode, and separate banks of control and status registers in Software mode.

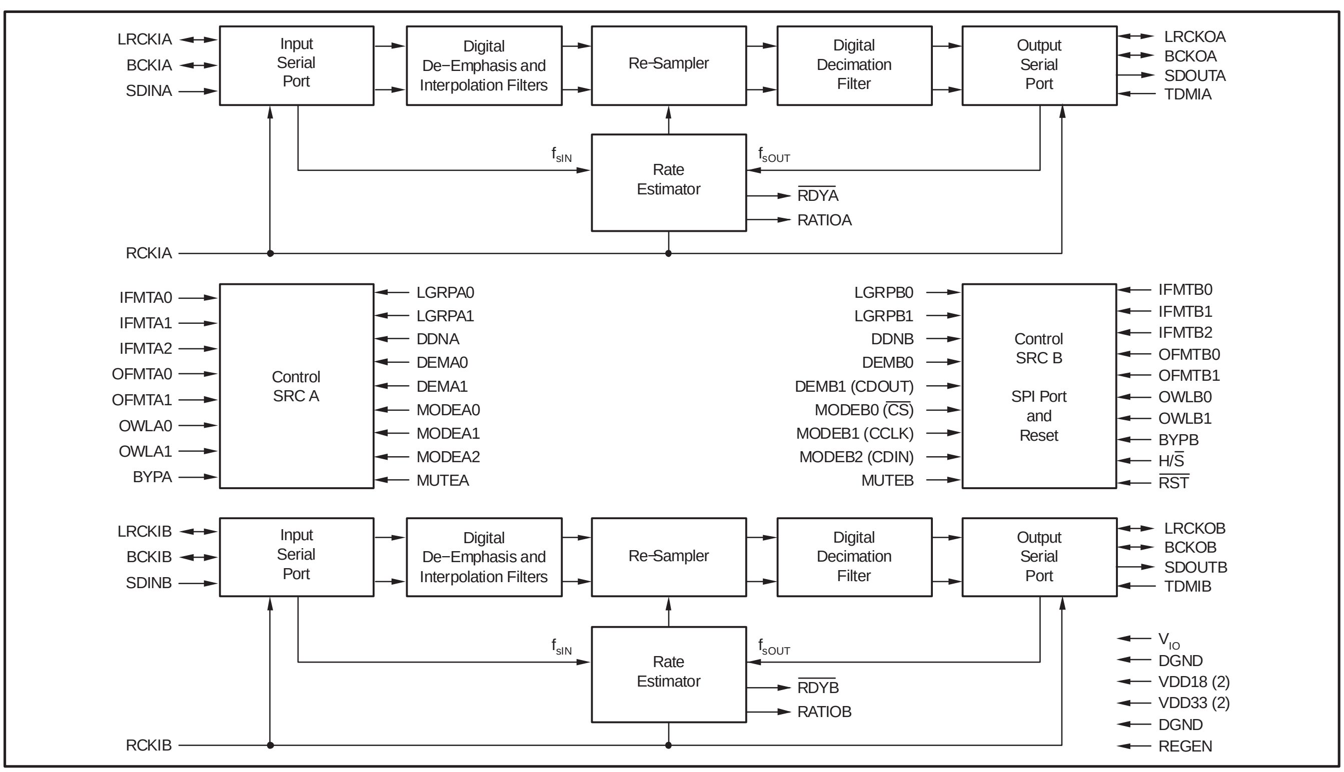


Figure 1. Functional Block Diagram

Operation for SRC A and SRC B is identical. Audio data is received at the input serial port, clocked by either the audio source device in Slave mode, or by the SRC4184 in Master mode. The output port data is clocked by either the audio output device in Slave mode, or by the SRC4184 in Master mode. The input data is passed through interpolation filters that upsample the data, which is then passed on to the re-sampler. The rate estimator compares the input and output sampling frequencies by comparing LRCKI, LRCKO, and a reference clock. The results of the rate estimation are utilized to configure the re-sampler coefficients and data pointers.

The output of the re-sampler is passed on to either the decimation filter or direct downsampler function. The decimation filter performs downsampling and anti-alias filtering functions, and is required when the output sampling frequency is equal to or lower than the input sampling frequency. The direct downsampler function does not provide any filtering, and may be used in cases when the output sampling frequency is greater than the input sampling frequency. The advantage of the direct downsampling function is a significant reduction in the group delay associated with the decimation function, allowing lower latency processing.

REFERENCE CLOCK

The SRC4184 includes two reference clock inputs, one each for SRC A and SRC B. The reference clocks are applied at the RCKIA (pin 20) and RCKIB (pin 29) inputs, respectively. The reference clock is required for the rate estimator function, as well as for the input or output serial ports when configured in Master mode.

Figure 2 illustrates the reference clock connections and requirements for the SRC4184. When either the input or output port is configured in Master mode, the reference clock may operate at $128f_S$, $256f_S$, or $512f_S$, where f_S is the desired sampling rate for the Master mode port. When both the input and output port are configured in Slave mode, the reference clock does not have to be a multiple of the input or output sampling rates. The maximum reference clock input frequency is 50MHz for RCKIA and RCKIB.

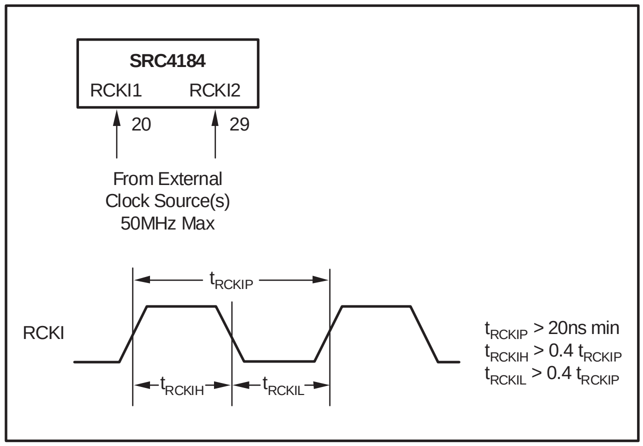


Figure 2. Reference Clock Input Connections and Timing Requirements

RESET AND POWER-DOWN OPERATION

The SRC4184 may be reset using the $\overline{RST}$ input (pin 21). There is no internal power-on reset, so the user should force a reset sequence after power-up in order to initialize the device. In order to force a reset, the reference clock inputs must be active, with external clock sources supplying a valid reference clock signal (refer to Figure 2). The user must assert $\overline{RST}$ low for a minimum of 500ns and then bring $\overline{RST}$ high again to force a reset. The reset function affects both SRC A and SRC B. Figure 3 shows the reset timing for the SRC4184.

In Software mode, there is a 500ms delay after the $\overline{RST}$ rising edge due to internal logic requirements. The customer should wait a minimum 500ms after the $\overline{RST}$ rising edge before attempting to write to the SPI port of the SRC4184 in Software mode.

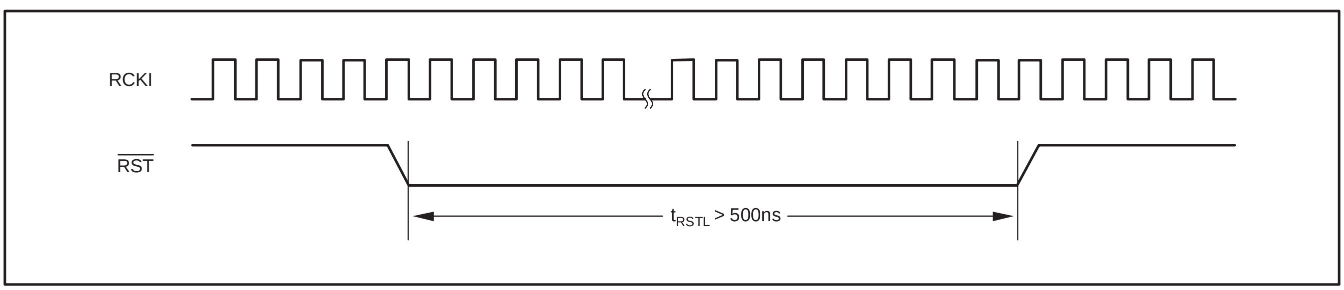


Figure 3. Reset Pulsewidth Requirement

The SRC4184 also supports two power-down modes. The entire SRC4184 may be powered down by forcing and holding the $\overline{RST}$ input low. This is referred to as a Hard Power-Down, and the SRC4184 consumes the least amount of power in this mode.

In Software mode, there is an additional Soft Power-Down available, utilizing the $\overline{PDN}$ bit in Control Register 1. Soft Power-Down is enabled when the $\overline{PDN}$ bit is set to 0. Since SRC A and SRC B have their own separate register banks, they may be set to Soft Power-Down mode individually. During Soft Power-Down, the SPI port and control registers remain active for write and read access. The internal voltage regulator also remains active if the REGEN pin is forced high and +3.3V is applied at the VDD33 pin.

Soft Power-Down mode consumes more power than the Hard Power-Down mode. Refer to the Electrical Characteristics tables in this data sheet for supply current and power dissipation specifications for both modes.

Finally, there is one very important item to remember when using Software mode. The default state of the $\overline{PDN}$ bit is 0, meaning that the SRC4184 will default to the Soft Power-Down state for both SRC A and SRC B after power-up or reset. The user must set the $\overline{PDN}$ bit to 1 for both the SRC A and SRC B control register banks in order to enable normal operation for both SRC sections.

AUDIO SERIAL PORT MODES

The SRC4184 supports seven serial port modes for the SRC A and SRC B sections, which are shown in Table 1. In Hardware mode, the audio port mode is selected using the MODEA0 (pin 14), MODEA1 (pin 15), and MODEA2 (pin 16) inputs for SRC A, while the MODEB0 (pin 35), MODEB1 (pin 34), and MODEB2 (pin 33) inputs are used for SRC B.

In Software mode, the audio serial port modes are selected using the MODE[2:0] bits in Control Register 1 for the SRC A and SRC B register banks. The default setting for Software mode is both input and output ports set to Slave mode.

In Slave mode, the port LRCK and BCK clocks are configured as inputs, and receive their clocks from an external audio device. In Master mode, the LRCK and BCK clocks are configured as outputs, being derived from the reference clock input for the corresponding SRC section, either RCKIA or RCKIB. Only one port can be set to Master mode at any given time, as indicated in Table 1.

Table 1. Setting the Serial Port Modes (x = A or B)

MODEx2	MODEx1	MODEx0	SERIAL PORT MODE
0	0	0	Both Input and Output Ports are Slave mode
0	0	1	Output Port is Master Mode with RCKIx = 128f_S
0	1	0	Output Port is Master Mode with RCKIx = 512f_S
0	1	1	Output Port is Master Mode with RCKIx = 256f_S
1	0	0	Both Input and Output Ports are Slave mode
1	0	1	Input Port is Master Mode with RCKIx = 128f_S
1	1	0	Input Port is Master Mode with RCKIx = 512f_S
1	1	1	Input Port is Master Mode with RCKIx = 256f_S

INPUT PORT OPERATION

The audio input port is a three-wire synchronous serial interface that may operate in either Slave or Master mode. The SDINA (pin 58) and SDINB (pin 55) are the serial audio data inputs for SRC A and SRC B, respectively. Audio data is input at these pins in one of three standard audio data formats: Philips I^2S, Left-Justified, or Right-Justified. The audio data word length may be up to 24-bits for I^2S and Left-Justified formats, while the Right-Justified format supports 16-, 18-, 20-, or 24-bit data. The audio data is always Binary Two's Complement with the MSB first. Refer to Figure 4 for the input data formats and Figure 5 for the critical timing parameters, which are also listed in the Electrical Characteristics table.

The bit clock is either an input or output at BCKIA (pin 60) and BCKIB (pin 53). In Slave mode, the bit clock is configured as an input pin, and may operate at rates from 32f_S to 128f_S,with a minimum of one clock cycle per data bit. In Master mode, bit clock operates at a fixed rate of 64f_S.

The left/right word clock, LRCKIA (pin 59) and LRCKIB (pin 54), may be configured as an input or output pin. In Slave mode, left/right clock is an input pin, while in Master mode the left/right clock is an output pin. In either case, the clock rate is equal to f_S, the input sampling frequency. The LRCKI duty cycle is fixed to 50% for Master mode operation.

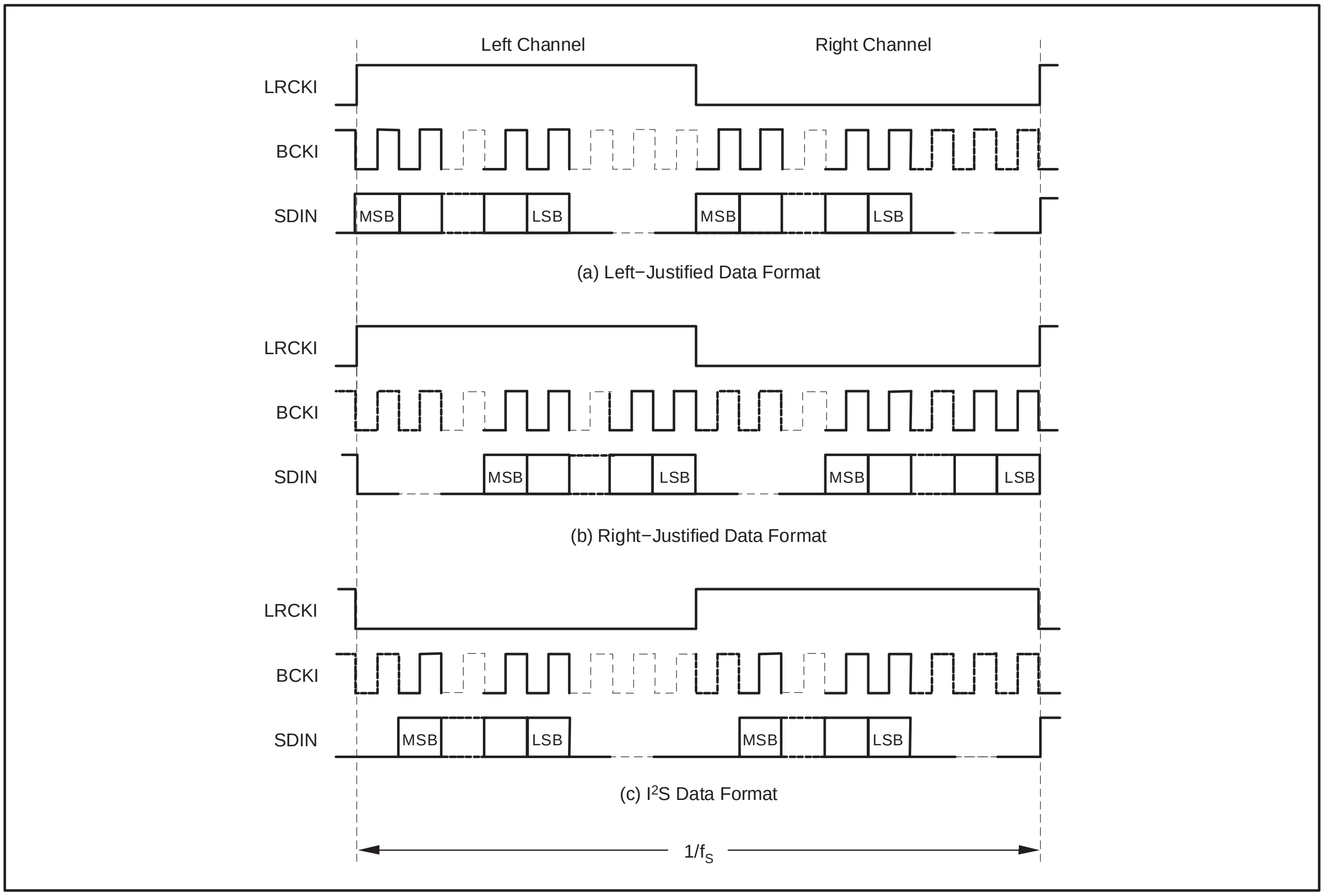


Figure 4. Input Data Formats

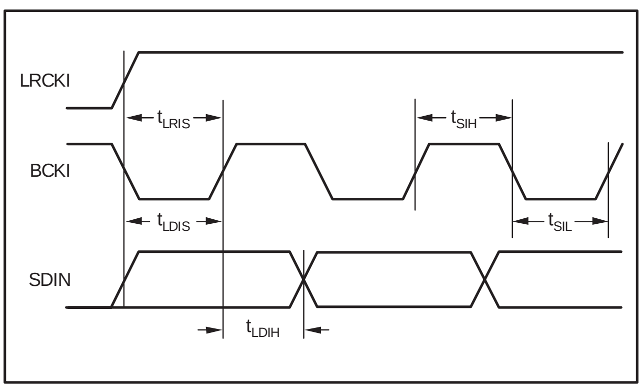


Figure 5. Input Port Timing

Table 2 illustrates the data format selection for the input port. For Hardware mode, the IFMTA0 (pin 1), IFMTA1 (pin 2), and IFMTA2 (pin 3) inputs are utilized to set the input port data format for SRC A. IFMTB0 (pin 48), IFMTB1 (pin 47), and IFMTB2 (pin 46) are utilized to set the input port data format for SRC B.

Table 2. Input Port Data Format Selection (x = A or B)

IFMTx2	IFMTx1	IFMTx0	INPUT PORT DATA FORMAT
0	0	0	24-Bit Left-Justified
0	0	1	24-Bit I^2S
0	1	0	Unused
0	1	1	Unused
1	0	0	16-Bit Right-Justified
1	0	1	18-Bit Right-Justified
1	1	0	20-Bit Right-Justified
1	1	1	24-Bit Right-Justified

In Software mode, the IFMT[2:0] bits in Control Register 3 are used to select the data format for the SRC A and SRC B register banks. The default format is 24-Bit Left-Justified.

OUTPUT PORT OPERATION

The audio output port is a four-wire synchronous serial interface that may operate in either Slave or Master mode. SDOUTA (pin 64) and SDOUTB (pin 49) are the serial audio data outputs for SRC A and SRC B, respectively. Audio data is output at these pins in one of four data formats: Philips I^2S, Left-Justified, Right-Justified, or TDM. The audio data word length may be 16-, 18-, 20-, or 24-bits. For all word lengths, the data is triangular PDF dithered from the internal 28-bit data path. The data formats (with the exception of TDM mode) are shown in Figure 7, while critical timing parameters are shown in Figure 6 and listed in the Electrical Characteristics table. The TDM format and timing are shown in Figure 15 and Figure 16, respectively, while examples of standard TDM configurations are shown in Figure 17 and Figure 18.

The bit clock is either input or output at BCKOA (pin 63) and BCKOB (pin 50). In Slave mode, the bit clock is configured as an input pin, and may operate at rates from $32f_S$ to $128f_S$, with a minimum of one clock cycle for each data bit. The exception is the TDM mode, where the BCKO must operate at $N \times 64f_S$, where N is equal to the number of SRC sections cascaded on the TDM bus. In Master mode, the bit clock operates at a fixed rate of $64f_S$ for all data formats except TDM, where BCKO operates at the reference clock frequency. Additional information regarding TDM mode operation is included in the *Applications Information* section of this data sheet.

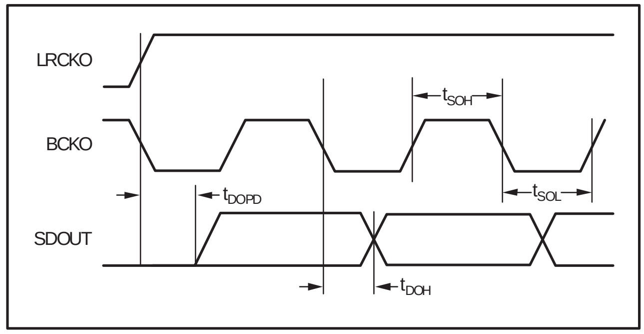


Figure 6. Output Port Timing

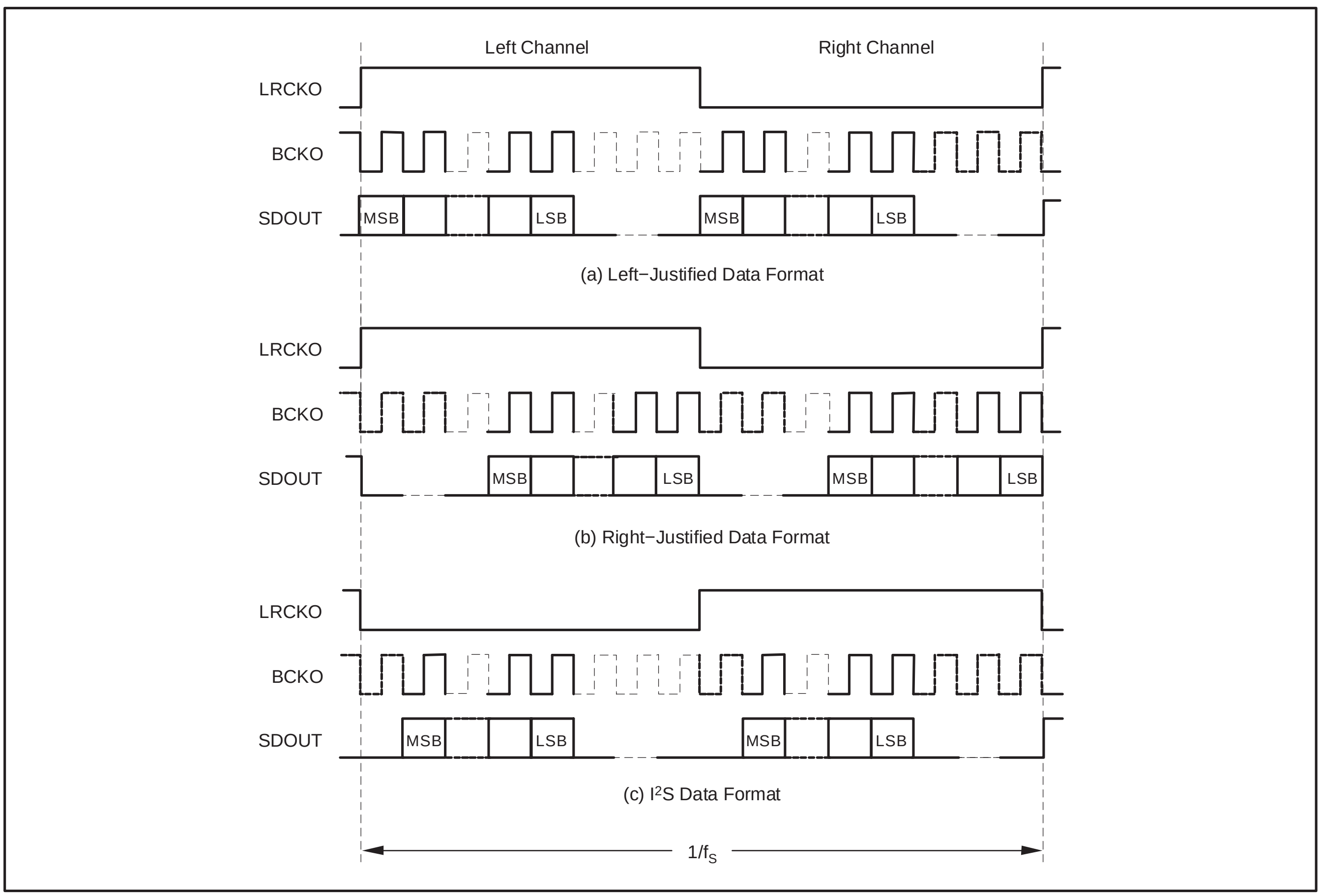


Figure 7. Output Data Formats

The left/right word clock, LRCKOA (pin 62) and LRCKOB (pin 51), may be configured as an input or output pin. In Slave mode, the left/right clock is an input pin, while in Master mode it is an output pin. In either case, the clock rate is equal to f_S, the output sampling frequency. The clock duty cycle is fixed to 50% for I^2S, Left-Justified, and Right-Justified formats in Master mode. The pulse width is fixed to 32-bit clock cycles for the TDM format in Master mode.

Table 3 illustrates data format selection for the output port. In Hardware mode, the OFMTA0 (pin 4), OFMTA1 (pin 5), OWLA0 (pin 6), and OWLA1 (pin 7) inputs are utilized to set the output port data format and word length for SRC A. The OFMTB0 (pin 45), OFMTB1 (pin 44), OWLB0 (pin 43), and OWLB1 (pin 42) inputs are utilized to set the output port data format and word length for SRC B.

Table 3. Output Port Data Format/Word Length Selection (x = A or B)

OFMTx1	OFMTx0	OUTPUT PORT DATA FORMAT
0	0	Left-Justified
0	1	I^2S
1	0	TDM
1	1	Right-Justified
OWLx1	**OWLx0**	**OUTPUT PORT DATA WORD LENGTH**
0	0	24 Bits
0	1	20 Bits
1	0	18 Bits
1	1	16 Bits

In Software mode, the OFMT[1:0] and OWL[1:0] bits in Control Register 3 are used to select the data format and word length for the SRC A and SRC B register banks. The default format is Left-Justified data with a default word length of 24-bits.

BYPASS MODE

The SRC4184 includes a bypass function for both SRC A and SRC B, which routes the input port data directly to the output port, bypassing the sample rate conversion block. Bypass mode may be invoked by forcing BYPA (pin 8) or BYPB (pin 41) high in either Hardware or Software mode. In Software mode, the bypass function may also be accessed using the BYPASS bit in Control Register 1 for the SRC A and SRC B register banks. For normal SRC operation, the bypass pins and control bits should be set to 0.

No dithering is applied to the output data in Bypass mode, and the digital attenuation, de-emphasis, and soft mute functions are also unavailable. Bypass mode is useful for passing through compressed or encoded audio data, as well as non-audio data (that is, control or status information).

INTERPOLATION FILTER GROUP DELAY OPTIONS

The SRC4184 provides four group delay options for the digital interpolation filter, as shown in Table 4. These options allow the user to tailor the group delay for a given application by selecting the number of input samples buffered prior to the re-sampling function.

Table 4. Low Group Delay Configuration (x = A or B)

LGRPx1	LGRPx0	BUFFER SIZE
0	0	64 Samples
0	1	32 Samples
1	0	16 Samples
1	1	8 Samples

In Hardware mode, the LGRPA0 (pin 9) and LGRPA1 (pin 10) inputs are used to select the group delay for SRC A, while LGRPB0 (pin 40) and LGRPB1 (pin 39) inputs are used for SRC B.

In Software mode, the LGRP[1:0] bits in Control Register 2 are used for the SRC A and SRC B register banks. The 64 sample buffer option is selected by default in Software mode.

DIRECT DOWNSAMPLING OPTION

The SRC4184 decimation function allows the selection of a direct downsampling option, as shown in Table 5. Unlike the decimation filter, the direct downsampler does not provide anti-alias filtering. This makes the direct downsampler suitable for applications where the output sample rate is higher than the input sample rate. The advantage of the direct downsampler is that there is no group delay associated with the decimation function.

Table 5. Decimation Function Configuration (x = A or B)

DDNx	DECIMATION FUNCTION
0	Decimation Filter Enabled
1	Direct Downsampler Enabled

In Hardware mode, the DDNA (pin 11) input is used to select the direct downsampler for SRC A, while the DDNB (pin 38) input is used for SRC B.

In Software mode, the DDN bit in Control Register 2 is used to select the direct downsampler for the SRC A and SRC B register banks. The decimation filter is selected by default, with direct downsampling disabled.

DIGITAL DE-EMPHASIS FILTER

The SRC4184 includes digital de-emphasis filtering following the input serial ports. The de-emphasis filter processes audio data that has been pre-emphasized using the 50/15µs transfer function, commonly used in consumer and professional audio systems. Pre-emphasis is utilized to increase the amplitude of the higher frequency components within the audio band. The de-emphasis filter normalizes the frequency response over the audio band.

The SRC4184 supports three sampling frequencies for the de-emphasis filter: 32kHz, 44.1kHz, and 48kHz. The de-emphasis filter can also be disabled. Table 6 shows the configuration table for the de-emphasis filter options.

Table 6. Digital De-Emphasis Filter Configuration (x = A or B)

DEMx1	DEMx0	DE-EMPHASIS FILTER FUNCTION
0	0	Disabled
0	1	48kHz Input Sample Rate
1	0	44.1kHz Input Sample Rate
1	1	32kHz Input Sample Rate

In Hardware mode, the DEMA0 (pin 12) and DEMA1 (pin 13) inputs are used to select the de-emphasis filter for SRC A, while DEMB0 (pin 37) and DEMB1 (pin 36) inputs are used for SRC B.

In Software mode, the DEM[1:0] bits in Control Register 2 are used to select the de-emphasis filter in both the SRC A and SRC B register banks. De-emphasis filtering is disabled by default in Software mode.

SOFT MUTE FUNCTION

The soft mute function of the SRC4184 may be invoked by forcing the MUTEA (pin 19) or MUTEB (pin 30) inputs high. In Software mode, the mute function may also be accessed using the MUTE bit in Control Register 1 for either the SRC A and SRC B register banks. The soft mute function slowly attenuates the output signal level down to an all zeros output. For normal output, the soft mute function should be disabled by forcing the control pin or bit low. The soft mute function is disabled by default in Software mode.

DIGITAL ATTENUATION
(Software Mode Only)

The SRC4184 includes independent digital attenuation for the Left and Right audio channels in Software mode. The attenuation ranges from 0dB (unity gain) to −127.5dB in 0.5dB steps. The attenuation settings are programmed using Control Register 4 and Control Register 5 for either the SRC A and SRC B register banks. The attenuation setting is programmed to 0dB (unity gain) by default.

The TRACK bit in Control Register 1 is used to select Independent or Tracking attenuation modes. When TRACK = 0, the Left and Right channels are controlled independently. When TRACK = 1, the attenuation setting for the Left channel is also used for the Right channel, providing a tracking function. The digital attenuation mode is set to Independent by default.

READY OUTPUT

The SRC4184 includes active low ready outputs for both SRC A and SRC B. The outputs are designated $\overline{\text{RDYA}}$ (pin 18) and $\overline{\text{RDYB}}$ (pin 31). The ready output is provided from the rate estimator block, with a low output state indicating that the input-to-output sampling frequency ratio has been determined and that the coefficients and address pointers for the re-sampling block have been updated. The ready signal may be used as a flag output for an external indicator or host.

RATIO OUTPUT

The SRC4184 includes a sampling ratio flag output for both SRC A and SRC B. The outputs are designated RATIOA (pin 17) and RATIOB (pin 32). When the ratio output is low, it indicates that the output sampling frequency is lower than the input sampling frequency. When ratio output is high, it indicates that the output sampling frequency is higher than the input sampling frequency. The ratio output can be used as a flag output for either an external indicator or host.

SAMPLING RATIO READBACK
(Software Mode Only)

In Software mode, Control Registers 6 and 7 in either the SRC A and SRC B register banks function as status registers, which contain the integer and fractional part of the input-to-output sampling ratio, or f_{SIN}:f_{SOUT}. Given that f_{SOUT} or f_{SIN} is known, the unknown sampling rate can be computed using the contents of Registers 6 and 7. This function may be useful for controlling end application display or control processes. Refer to the *Control Register Definition* section of this datasheet for additional information regarding Registers 6 and 7.

SERIAL PERIPHERAL INTERFACE (SPI) PORT
(Software Mode Only)

The SPI port is a four-wire synchronous serial interface used to access the on-chip control registers of the SRC4184. The interface is comprised of a serial data clock input, CCLK (pin 34); a serial data input, CDIN (pin 33); a serial data output, CDOUT (pin 36); and an active low chip-select input, $\overline{\text{CS}}$ (pin 35). The CDOUT pin is a tri-state output and is forced to a high impedance state when the $\overline{\text{CS}}$ input is forced high.

Figure 8 illustrates the protocol for register write and read operations via the SPI port. Figure 9 shows the critical timing parameters for the SPI port interface, which are listed in the Electrical Characteristics table.

Byte 0 indicates the register bank, register address, and read/write status for the operation. The functions contained within this byte are clearly shown in Figure 8. It should be noted that either one or both of the SRC A and SRC B register banks may be written to in the same operation, but only one bank can be selected at any time for a read operation. Byte 1 is a *don't care* byte. This byte is included in the protocol in order to maintain compatibility with current and future Texas Instruments' digital audio interface products, including the DIT4096, DIT4192, and SRC4193. Bytes 0 and 1 are followed by register data bytes.

As shown in Figure 8, a write or read operation starts by bringing the $\overline{CS}$ input low. Bytes 0, 1, and 2 are then written to write or read a single register. Byte 2 is not needed for reading registers, so the CDIN pin can be forced low after Byte 0 for a read operation. Bringing the $\overline{CS}$ input high after the third byte will write or read a single register address. However, if $\overline{CS}$ remains low after writing or reading the first control or status byte, the port will automatically increment the address by 1, allowing successive addresses to be written or read sequentially. The address is automatically incremented by 1 after each byte is written or read, as long as the $\overline{CS}$ input remains low. This is referred to as Auto-Increment operation, and is always enabled for the SPI port.

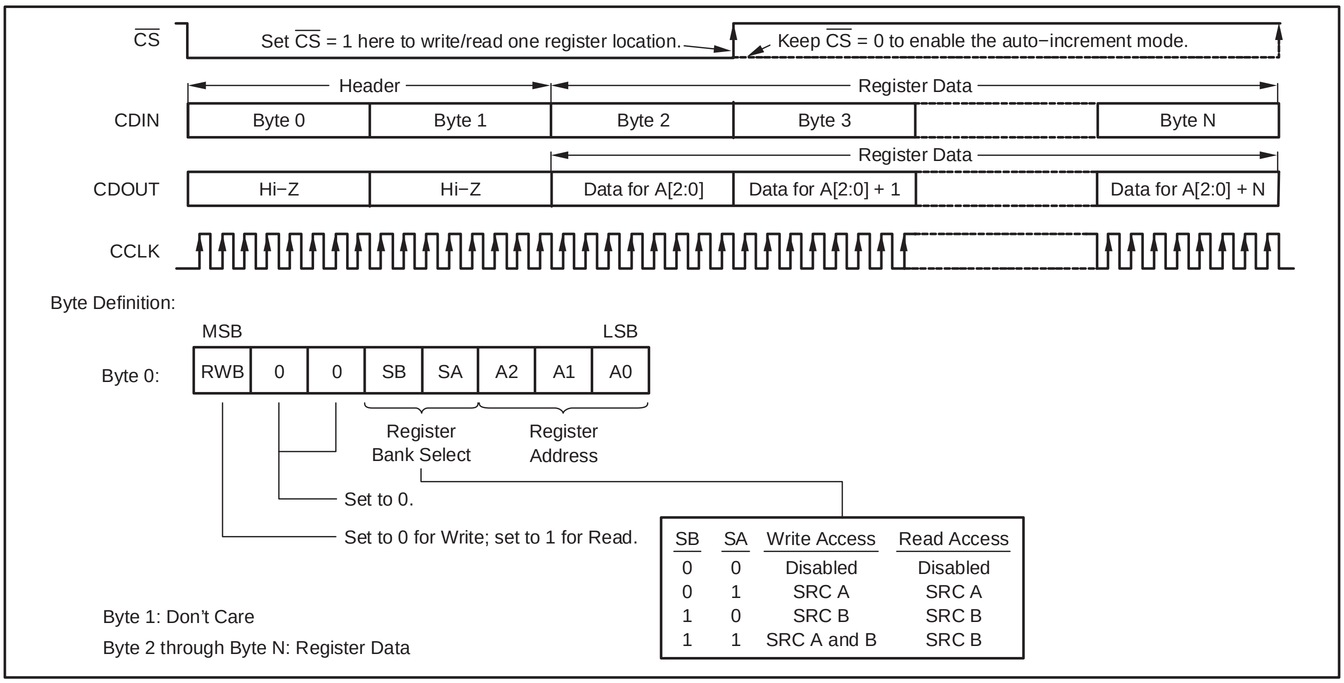


Figure 8. SPI Protocol for the SRC4184

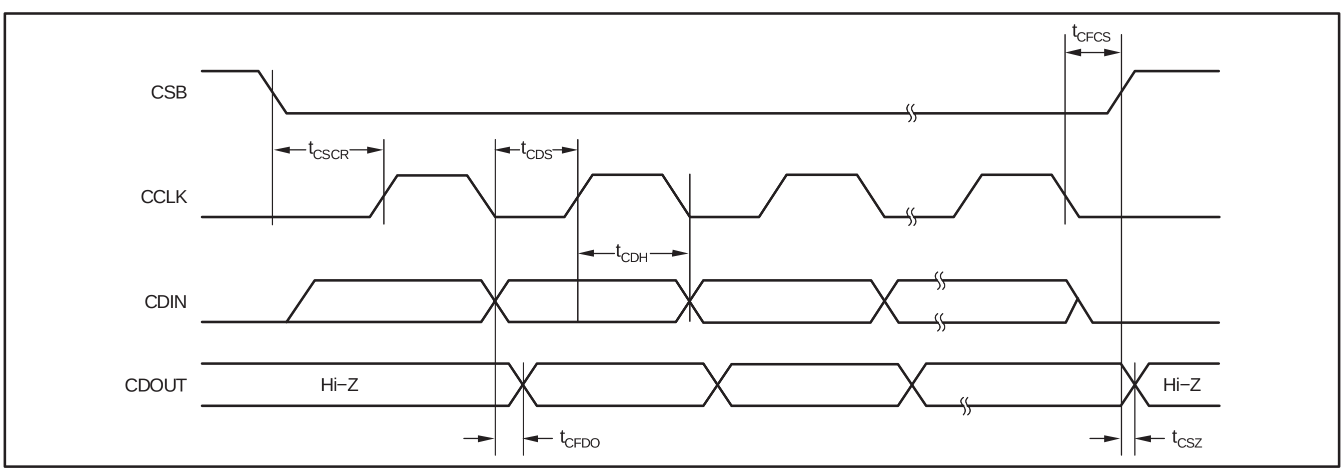


Figure 9. SPI Port Timing

CONTROL REGISTER MAP

(Software Mode Only)

The control register map for the SRC4184 is shown in Table 7. There are two identical register banks, one for SRC A and one for SRC B, each conforming to the register map shown in Table 7.

Register 0 is reserved for factory use and defaults to all zeros upon reset. The user should avoid writing to or reading this register, as unexpected operation may result if Register 0 is programmed to an arbitrary value.

Register 1 through Register 5 contain control bits, which are programmed to configure specific internal functions. Register 1 through Register 5 are available for write or read access. Register 6 and Register 7 contain the integer and fractional parts of the f_{SIN}:f_{SOUT} sampling ratio and are read only status registers.

Table 7. Control Register Map for Either the SRC A or SRC B Register Banks

REGISTER ADDRESS (HEX)	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0
1	$\overline{\text{PDN}}$	TRACK	0	MUTE	BYPASS	MODE2	MODE1	MODE0
2	0	0	0	DEM1	DEM0	DDN	LGRP1	LGRP0
3	OWL1	OWL0	OFMT1	OFMT0	0	IFMT2	IFMT1	IFMT0
4	AL7	AL6	AL5	AL4	AL3	AL2	AL1	AL0
5	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0
6	SRI4	SRI3	SRI2	SRI1	SRI0	SRF10	SRF9	SRF8
7	SRF7	SRF6	SRF5	SRF4	SRF3	SRF2	SRF1	SRF0

CONTROL REGISTER DEFINITIONS

(Software Mode Only)

This section contains descriptions for each control and status register available in Software mode. Reset defaults are also shown for each register bit.

Register 1. System Control Register

D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
$\overline{PDN}$	TRACK	0	MUTE	BYPASS	MODE2	MODE1	MODE0

MODE[2:0] **Audio Serial Port Mode**

These bits are used to select the Slave or Master mode status of the input and output serial ports.

MODE2	MODE1	MODE0	AUDIO SERIAL PORT MODE
0	0	0	Both Serial Ports are in Slave Mode (default)
0	0	1	Output Serial Port is Master with RCKI = $128f_S$
0	1	0	Output Serial Port is Master with RCKI = $512f_S$
0	1	1	Output Serial Port is Master with RCKI = $256f_S$
1	0	0	Both Serial Ports are in Slave Mode
1	0	1	Input Serial Port is Master with RCKI = $128f_S$
1	1	0	Input Serial Port is Master with RCKI = $512f_S$
1	1	1	Input Serial Port is Master with RCKI = $256f_S$

BYPASS **Bypass Mode**

This bit is logically OR'd with the bypass input (BYPA or BYPB) for the corresponding SRC section.

BYPASS	FUNCTION
0	Bypass Mode disabled with normal ASRC operation. (default)
1	Bypass Mode enabled with data routed directly from the input port to the output port, bypassing the ARSC function.

MUTE **Output Soft Mute**

This bit is logically OR'd with the MUTE input (MUTEA or MUTEB) for the corresponding SRC section.

MUTE	OUTPUT MUTE FUNCTION
0	Soft mute disabled. (default)
1	Soft mute enabled with output data attenuated to all 0s

TRACK **Digital Attenuation Tracking**

TRACK	ATTENUATION TRACKING
0	Tracking Off: Attenuation for the Left and Right channels is controlled independently by Control Register 4 and Control Register 5. (default)
1	Tracking On: Left channel attenuation setting is used for both channels.

$\overline{PDN}$ **Power-Down**

Setting this bit to 0 will force the corresponding SRC section into Soft Power-Down mode. All other register settings are preserved and the SPI port remains active. Setting this bit to 1 will power-up the corresponding SRC section using the current register settings.

This bit defaults to 0 on power-up or reset. It must be programmed to 1 by the user in order to enable normal operation for the corresponding SRC section.

Register 2. Digital Filter Control Register

D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
0	0	0	DEM1	DEM0	DDN	LGRP1	LGRP0

LGRP0 **Interpolation Filter Group Delay**

LGRP1 These bits are used to select the number of input samples to be stored in the data buffer before the re-sampler starts to process the data. This has a direct impact on the group delay or latency of the interpolation filter.

LGRP1	LGRP0	GROUP DELAY
0	0	64 Samples (default)
0	1	32 Samples
1	0	16 Samples
1	1	8 Samples

DDN **Decimation Filtering/Direct DownSampling**

The DDN bit is used to enable or disable the direct downsampling function of the decimation block.

DDN	DECIMATION FILTER OPERATION
0	Decimation filter enabled. (default) (Must be used when f_{SOUT} is less than or equal to f_{SIN}.)
1	Direct downsampling enabled without filtering. (May be enabled when f_{SOUT} is greater than f_{SIN}.)

DEM0 **Digital De-Emphasis Filtering**

DEM1 These bits are used to configure the digital de-emphasis filter function.

DEM1	DEM0	DE-EMPHASIS FILTER
0	0	Disabled (default)
0	1	48kHz Input Sampling Rate
1	0	44.1kHz Input Sampling Rate
1	1	32kHz Input Sampling Rate

Register 3. Audio Data Format Register

D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
OWL1	OWL0	OFMT1	OFMT0	0	IFMT2	IFMT1	IFMT0

IFMT[2:0] Input Serial Port Data Format

These bits are utilized to select the audio data format for the input serial port.

IFMT2	IFMT1	IFMT0	INPUT FORMAT
0	0	0	24-Bit, Left-Justified (default)
0	0	1	24-Bit, I^2S
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Right-Justified, 16-Bit Data
1	0	1	Right-Justified, 18-Bit Data
1	1	0	Right-Justified, 20-Bit Data
1	1	1	Right-Justified, 24-Bit Data

OFMT[1:0] Output Port Data Format

These bits are utilized to select the audio data format for the output serial port.

OFMT1	OFMT0	OUTPUT FORMAT
0	0	Left-Justified (default)
0	1	I^2S
1	0	TDM
1	1	Right-Justified

OWL[1:0] Output Port Data Word Length

OWL1	OWL0	OUTPUT WORD LENGTH
0	0	24-Bits (default)
0	1	20-Bits
1	0	18-Bits
1	1	16-Bits

Register 4. Digital Output Attenuation Register—Left Channel

D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
AL7	AL6	AL5	AL4	AL3	AL2	AL1	AL0

This register is utilized to program the digital output attenuation for the Left output channel of the corresponding SRC section.

Register defaults to 00h, or 0dB (unity gain).

Output Attenuation (dB) = $-N \times 0.5$, where N = $AL[7:0]_{DEC}$

Register 5. Digital Output Attenuation Register—Right Channel

D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0

This register is utilized to program the digital output attenuation for the Right output channel of the corresponding SRC section. When the TRACK bit in Control Register 1 is set to 1, the Left Channel attenuation setting will also be used to set the Right Channel attenuation.

Register defaults to 00h, or 0dB (unity gain).

Output Attenuation (dB) = $-N \times 0.5$, where N = $AR[7:0]_{DEC}$

Register 6. Sampling Ratio (read only)

D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
SRI4	SRI3	SRI2	SRI1	SRI0	SRF10	SRF9	SRF8

Register 7. Sampling Ratio (read only)

D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
SRF7	SRF6	SRF5	SRF4	SRF3	SRF2	SRF1	SRF0

The contents of Register 6 and Register 7 indicate the input-to-output sampling ratio, and can be used to determine either the input or output sampling rates when one of the two rates is known.

Bits SRI[4:0] comprise the integer portion of the input-to-output sampling ratio.

Bits SRF[10:0] comprise the fractional portion of the input-to-output sampling ratio.

The contents of Register 6 and Register 7 are updated when Register 6 is read. Register 6 must always be read first in order to obtain the latest ratio data for both registers.

APPLICATIONS INFORMATION

This section provides practical applications information for hardware and systems engineers who will be designing the SRC4184 into their end equipment.

TYPICAL CONNECTIONS

Figure 10 and Figure 11 illustrate typical connection diagrams for Hardware and Software modes, respectively. In Hardware mode, dedicated pins are controlled using external logic circuitry, hardwiring pins high or low, or by using the general-purpose I/O pins of a microprocessor or DSP. In Software mode, the SRC4194 is controlled via the 4-wire SPI port and optional GPIO from either a microprocessor or DSP.

Figure 12 illustrates the power-supply options for the SRC4194. When utilizing +3.3V for the core supply, the REGEN input (pin 26) must be driven high in order to enable the on-chip linear voltage regulator. The VDD33 pins are supplied with +3.3V and the VDD18 pins are left unconnected.

Recommended power supply bypass capacitor values are shown in Figure 10 through Figure 12. Ceramic capacitors (X7R chip type) are recommended for the 0.1μF capacitors, while the 10μF capacitors may be tantalum or multi-layer X7R ceramic chip type, or through-hole or surface mount aluminum electrolytic capacitors.

When utilizing +1.8V for the core supply, the REGEN input (pin 26) must be driven low in order to disable the on-chip linear voltage regulator. The VDD18 pins are supplied with +1.8V and the VDD33 pins are left unconnected.

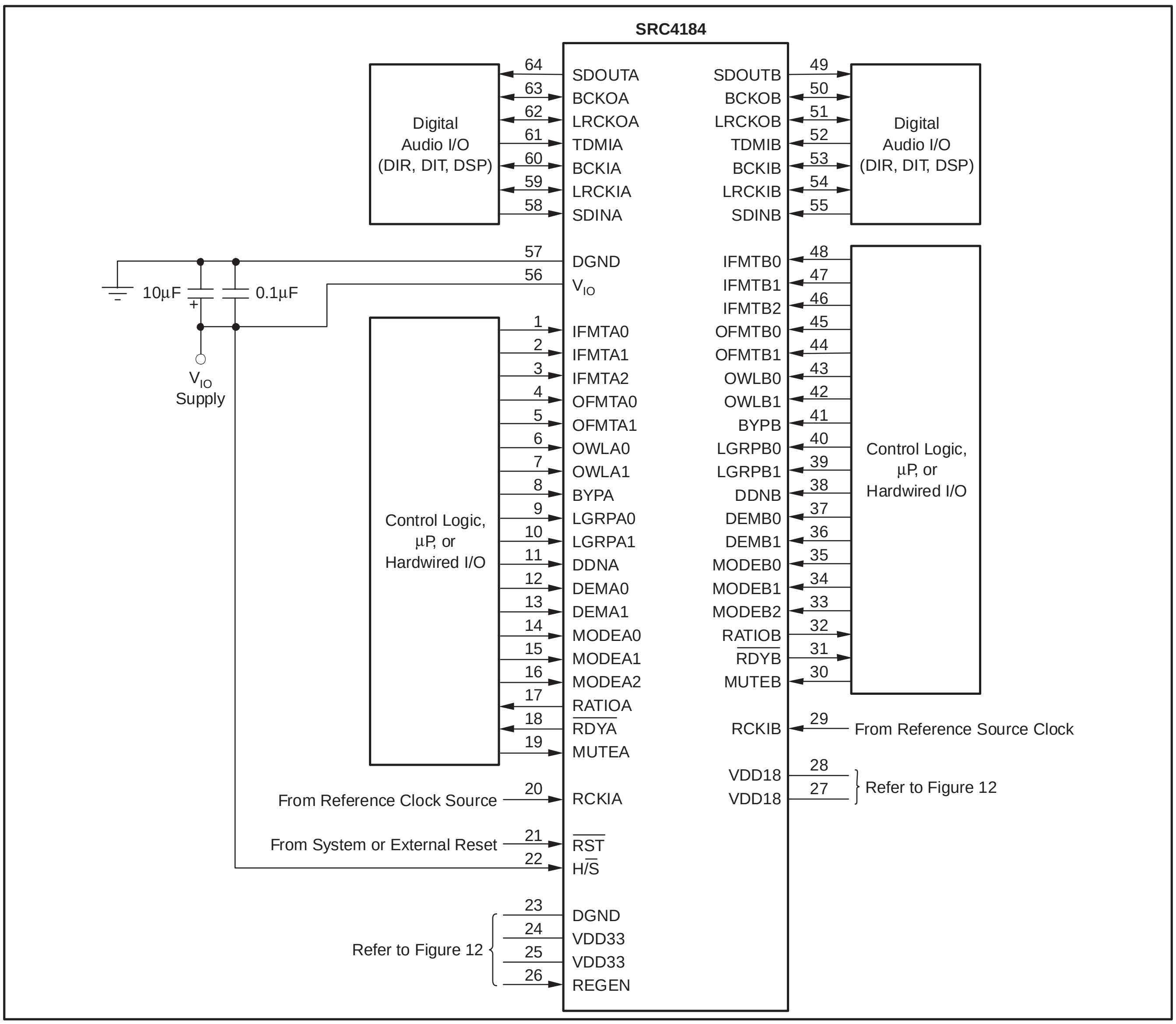


Figure 10. Typical Pin Connections for Hardware Mode Operation

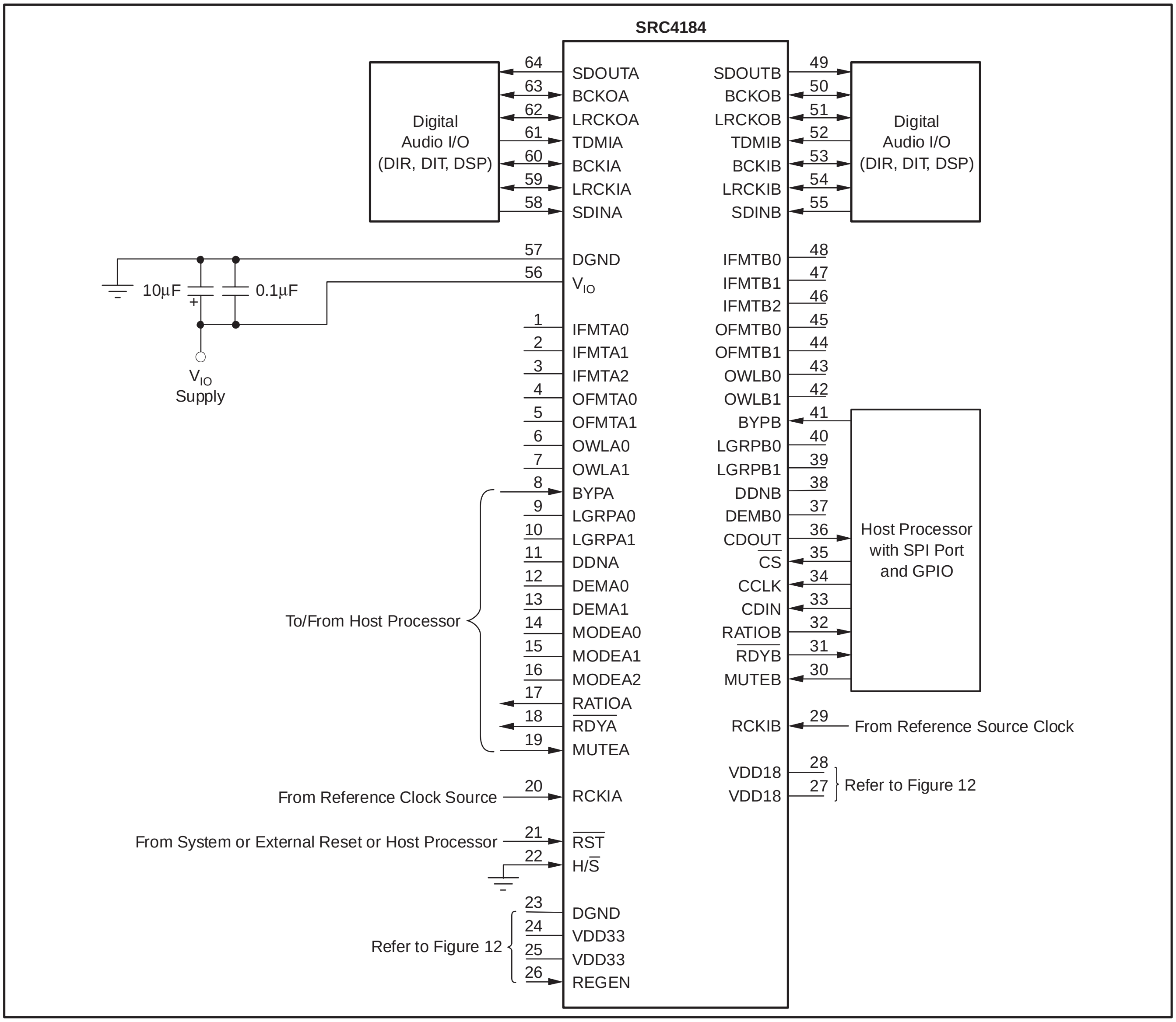


Figure 11. Typical Pin Connections for Software Mode Operation

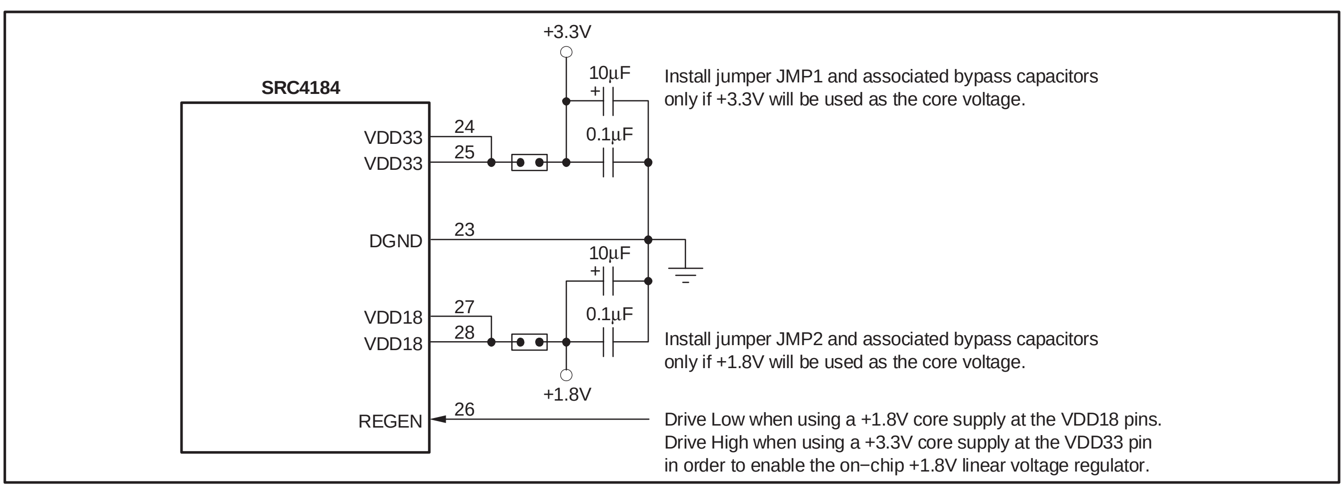


Figure 12. Core Power-Supply Connection Options

INTERFACING TO DIGITAL AUDIO RECEIVERS AND TRANSMITTERS

The SRC4184 input and output ports are designed to interface to a variety of audio devices, including receivers and transmitters commonly used for AES/EBU, S/PDIF, and CP1201 communications. Texas Instruments manufactures the DIR1703 digital audio interface receiver and DIT4096/4192 digital audio transmitters to address these applications.

Figure 13 illustrates interfacing the DIR1703 to the SRC4184 input port. The DIR1703 operates from a single +3.3V supply, which requires that the V_{IO} supply (pin 56) for the SRC4184 to be set to +3.3V for interface compatibility.

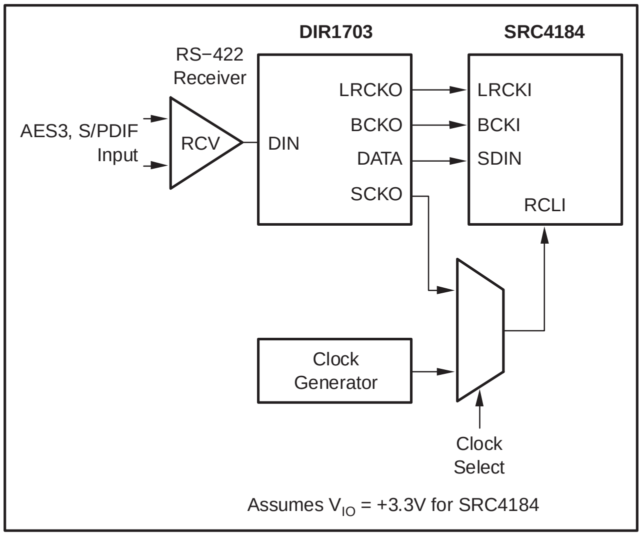


Figure 13. Interfacing the SRC4184 to the DIR1703 Digital Audio Interface Receiver

Figure 14 shows the interface between the SRC4184 output port and the DIT4096 or DIT4192 audio serial port. Once again, the V_{IO} supplies for both the SRC4184 and DIT4096/4192 are set to +3.3V for interface compatibility.

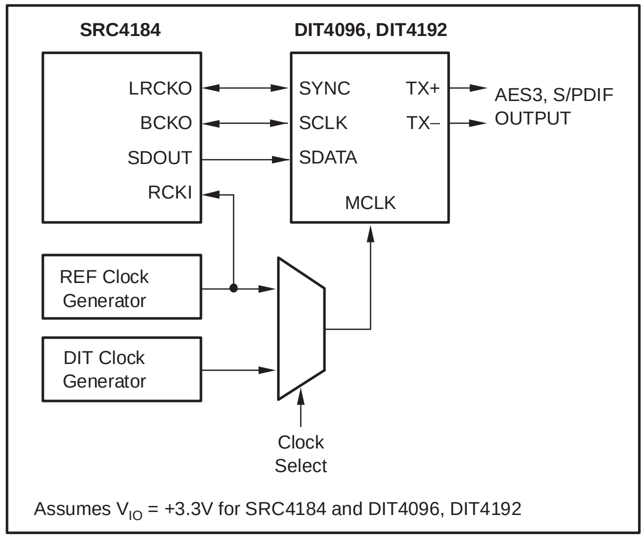


Figure 14. Interfacing the SRC4184 to the DIT4096/4192 Digital Audio Interface Receiver

Like the SRC4184 output ports, the DIT4096 and DIT4192 audio serial port may be configured as a Master or Slave. In cases where the SRC4184 output port is set to Master mode and the DIT4096/4192 is configured as the Slave, it is recommended to use the reference clock source for the corresponding section of the SRC4184 as the master clock source for the DIT4096/4192. This will ensure that the transmitter audio serial port clocks, SYNC and SCLK, are synchronized to the master clock source.

TDM APPLICATIONS

The SRC4184 supports a TDM output mode, which allows multiple devices to be daisy-chained together to create a serial frame. Each device occupies one sub-frame within a frame, and each sub-frame carries two channels (Left followed by Right). Each sub-frame is 64 bits long, with 32 bits allotted for each channel. The audio data for each channel is left-justified within the allotted 32 bits. Figure 16 illustrates the TDM frame format, while Figure 15 shows TDM input timing parameters, which are listed in the Electrical Characteristics table of this data sheet.

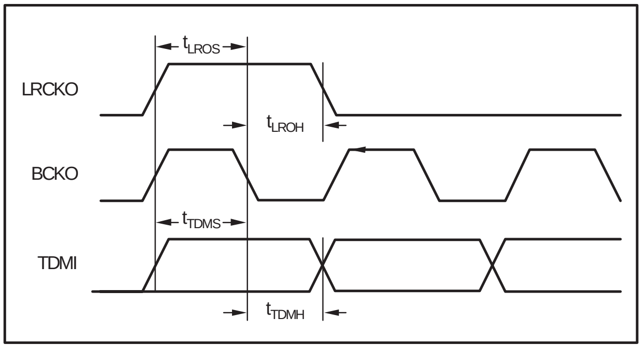


Figure 15. Input Timing for TDM Mode

The frame rate is equal to the output sampling frequency, f_S. The BCKO frequency for the TDM interface is $N \times 64f_S$, where N is the number of SRC sections included in the daisy-chain. For Master mode, the output BCKO frequency is fixed to the reference clock input frequency. The number of devices that can be daisy-chained in TDM mode is dependent upon the output sampling frequency and the bit clock frequency, leading to the following numerical relationship:

Number of Daisy-Chained SRC Sections = $(f_{BCKO}/f_S)/64$

Where:

f_{BCKO} = Output Port Bit Clock (BCKO), 27MHz maximum

f_S = Output Port Sampling (or LRCKO) Frequency, 212kHz maximum.

This relationship holds true for both Slave and Master modes.

Figure 17 and Figure 18 illustrate typical connection schemes for TDM mode. Although the TMS320C671x DSP family is shown as the audio processing engine in these figures, other TI digital signal processors with a multi-channel buffered serial port (McBSP™) may also function with this arrangement. Interfacing to processors from other manufacturers is also possible. Refer to the timing diagrams this data sheet, along with the equivalent serial port timing diagrams shown in the DSP data sheet to determine compatibility.

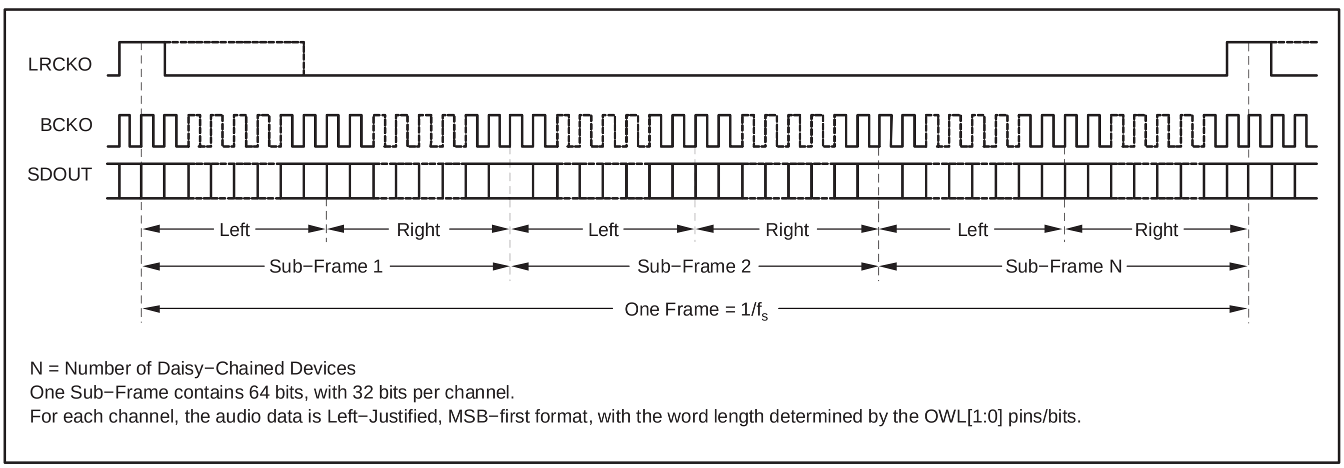


Figure 16. TDM Frame Format

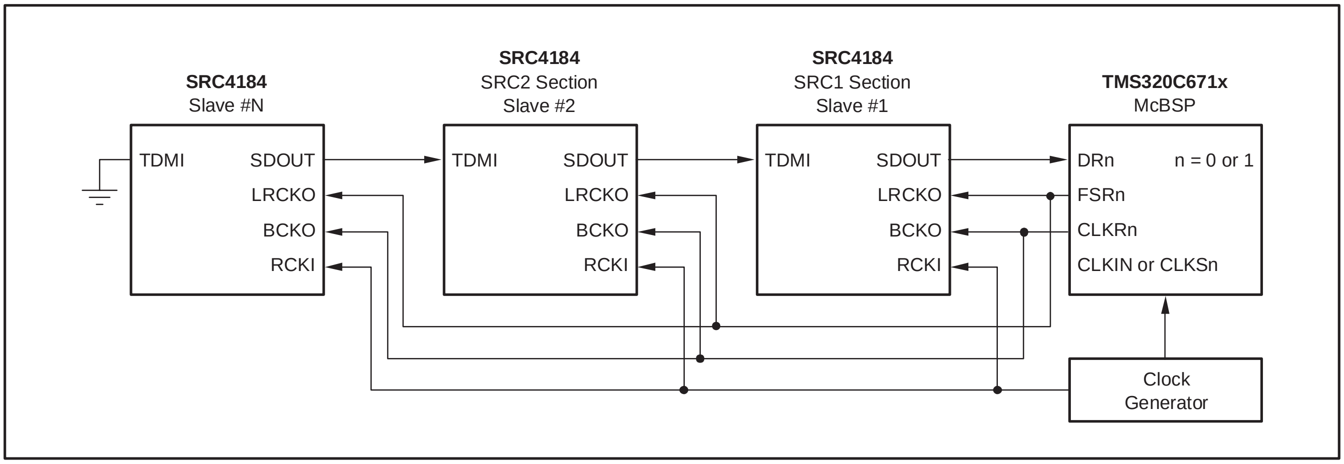


Figure 17. TDM Interface where All Devices are Slaves

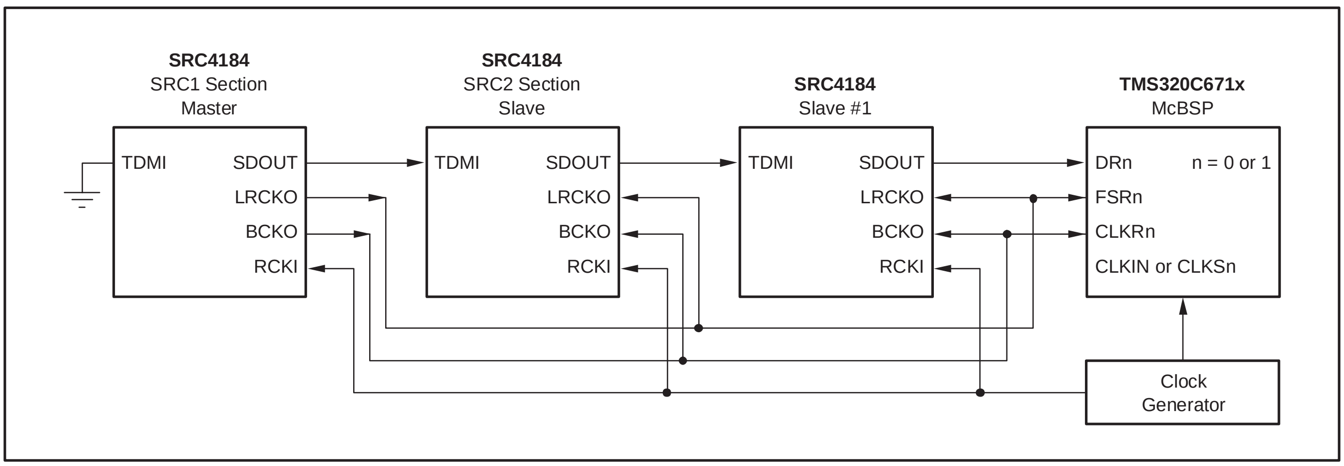


Figure 18. TDM Interface where One Device is Master to Multiple Slaves

Revision History

DATE	REV	PAGE	SECTION	DESCRIPTION
9/07	B	1	Front Page	Added U.S. patent number.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SRC4184IPAG	ACTIVE	TQFP	PAG	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR
SRC4184IPAGG4	ACTIVE	TQFP	PAG	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR
SRC4184IPAGR	ACTIVE	TQFP	PAG	64	1500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR
SRC4184IPAGRG4	ACTIVE	TQFP	PAG	64	1500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR
SRC4184IPAGT	ACTIVE	TQFP	PAG	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR
SRC4184IPAGTG4	ACTIVE	TQFP	PAG	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

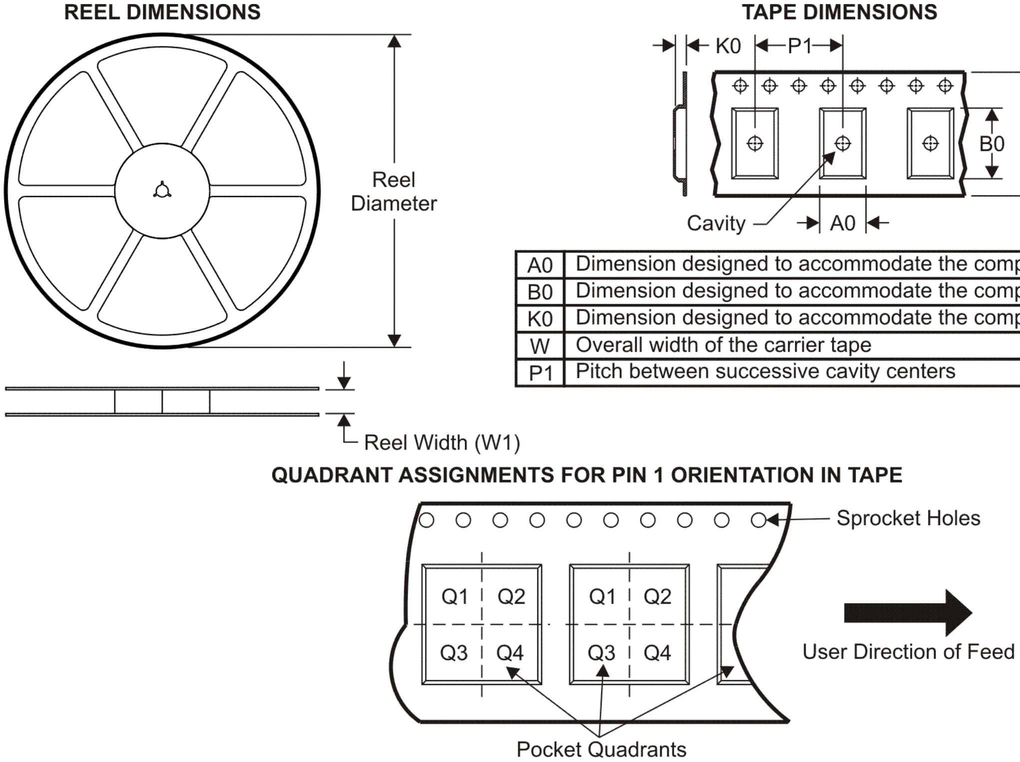
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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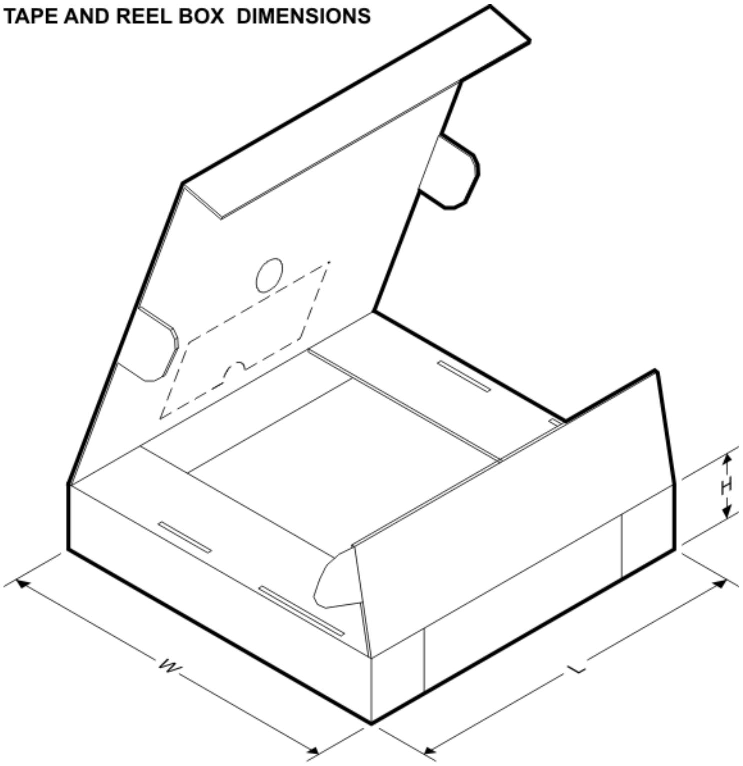


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SRC4184IPAGR	TQFP	PAG	64	1500	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2
SRC4184IPAGT	TQFP	PAG	64	250	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2

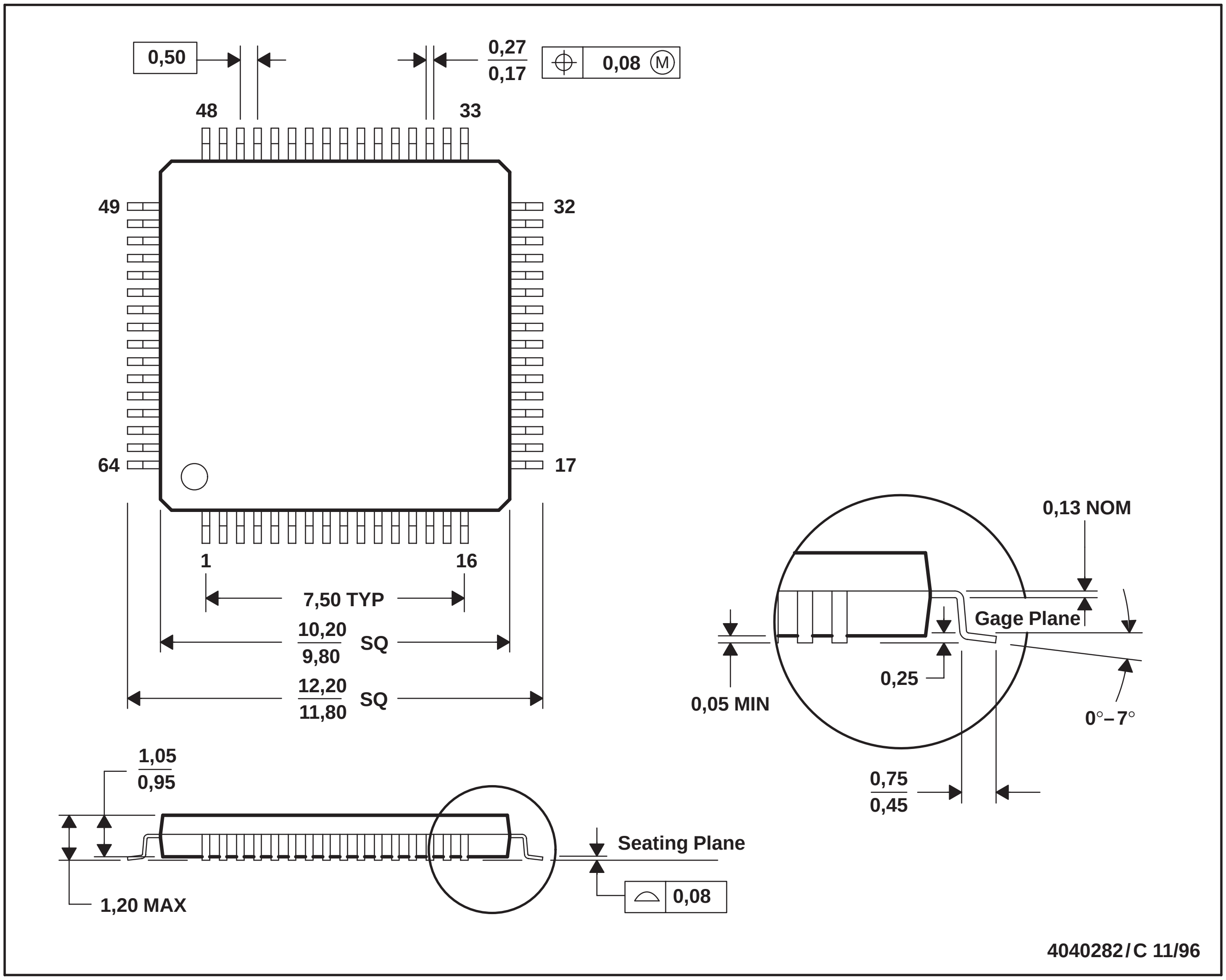
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SRC4184IPAGR	TQFP	PAG	64	1500	346.0	346.0	41.0
SRC4184IPAGT	TQFP	PAG	64	250	346.0	346.0	41.0

PAG (S-PQFP-G64) PLASTIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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